


Redwood BSW 11.6" Schematic Document

Braswell

2015-03-27
REV : A00

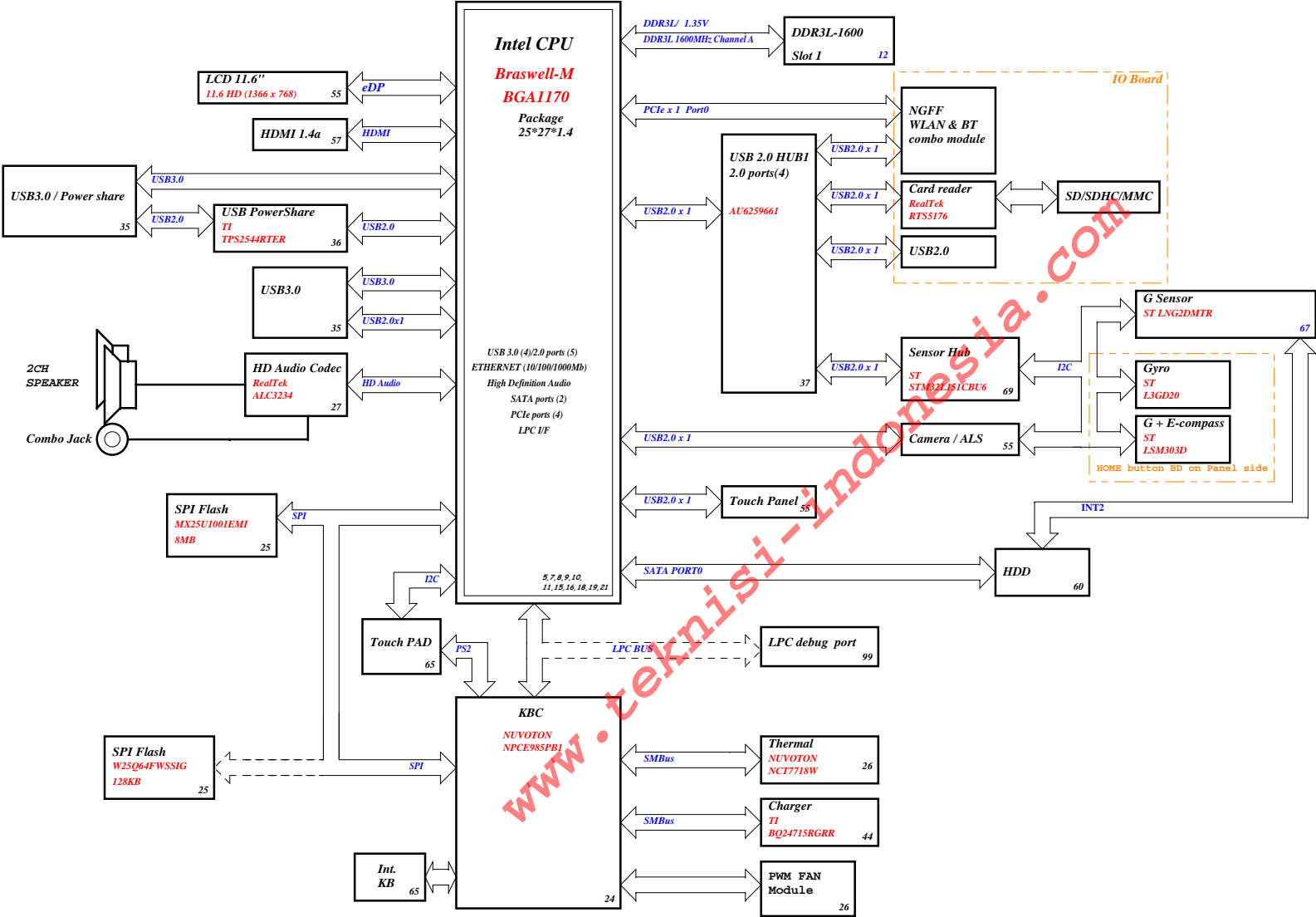
DY : None Installed
XDP: For CPU XDP Debug Port installed
APS: For Intel Auto Power Switch Debug Port
Share/nonS: Share ROM or Non Share ROM

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Title			
Cover Page			
Size A3	Document Number Redwood BSW 11.6"		Rev A00
Date: Thursday, March 19, 2015		Sheet 1	of 109

Project code : 4PD04K010001
PCB P/N : 14274
Revision : -1

Redwood BSW 11.6" Board Block Diagram



CHARGER	
BQ24715RGRR	44
INPUTS	OUTPUTS
19V_AD+	12V_BT+
SYSTEM DC/DC	
TPS51225	45
INPUTS	OUTPUTS
19V_DCBATOUT	3D3V_AUX_S5
	3D3V_S5
	5V_S5
CPU DC/DC	
NCP81201MNTXG	46-47
INPUTS	OUTPUTS
19V_DCBATOUT	1V_CPU_CORE
CPU DC/DC	
NCP81201MNTXG	48
INPUTS	OUTPUTS
19V_DCBATOUT	6FX_CORE
SYSTEM DC/DC	
SY8208DQNC	50
INPUTS	OUTPUTS
19V_DCBATOUT	1D05V_S5
Step Down Regulator	
TLV70218	50
INPUTS	OUTPUTS
3D3V_S5	1D15V_S5
SYSTEM DC/DC	
SY8206DQNC	51
INPUTS	OUTPUTS
19V_DCBATOUT	1D35V_CPU_VDDQ_S3
SYSTEM DC/DC	
APL5338XAI	51
INPUTS	OUTPUTS
1D35V_CPU_VDDQ_S3	0D675V_VREF_S0
Step Down Regulator	
SYW232DFC	52
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5
SYSTEM LDO	
S-1339D15-M5001	53
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
SYSTEM LDO	
APL5930KAI	54
INPUTS	OUTPUTS
3D3V_S5	1D24V_S5

PCB LAYER	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

SSID = CPU

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Rev
A00

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Sheet 3 of 109

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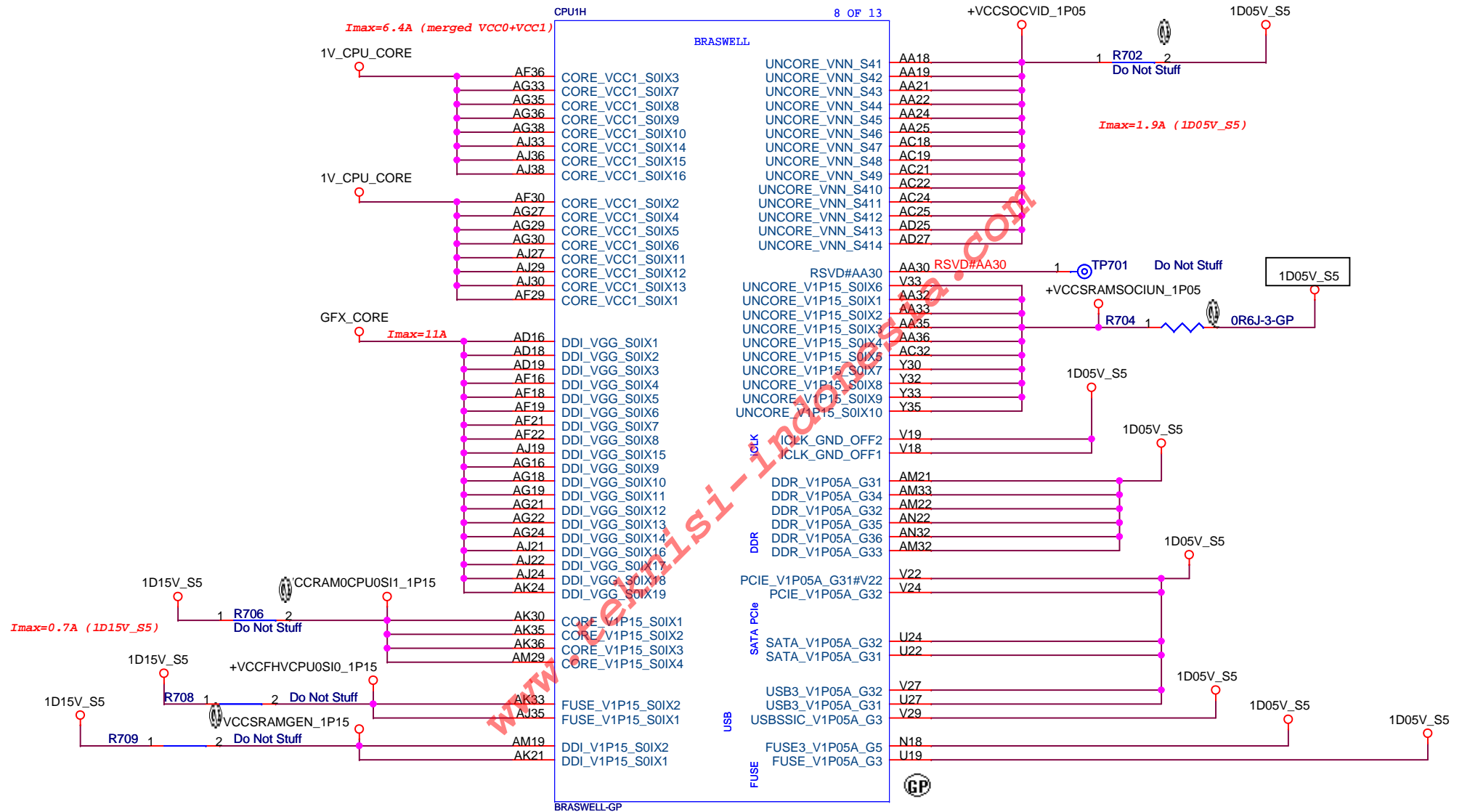
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Date: Thursday, March 19, 2015		Sheet 6 of	109

SSID = CPU



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CPU (VCC CORE)

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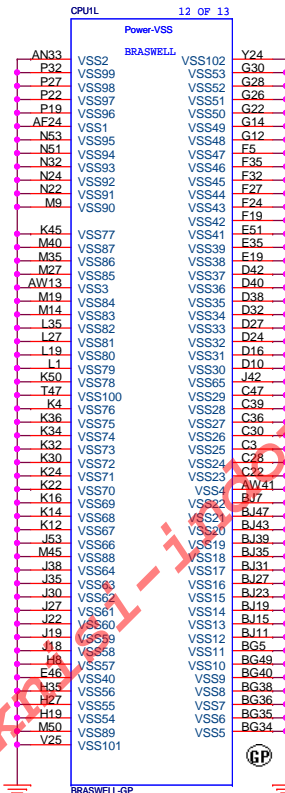
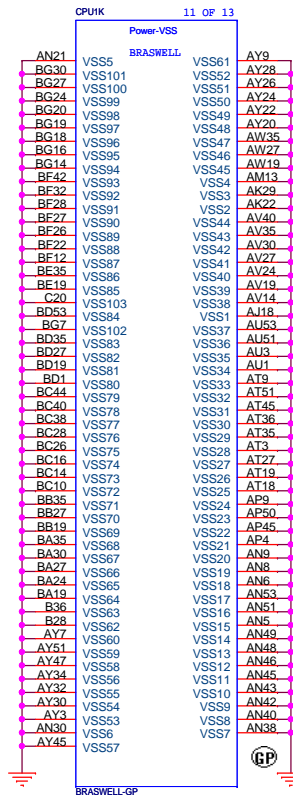
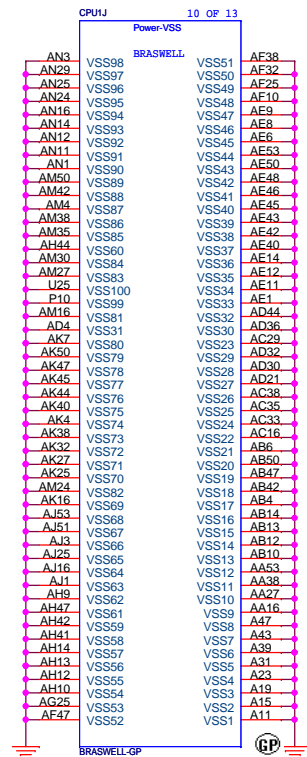
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Rev
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Date: Wednesday, March 25, 2015

Sheet 7 of 109

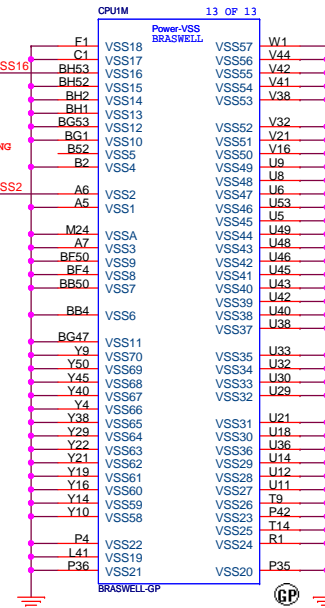
SSID = CPU



2014/04/25
Intel suggest
TP901 1
Do Not Stuff

B52 MAY NOT BE ABLE TO BREAK OUT IN ROUTING

2014/04/25
Intel suggest
TP902 1
Do Not Stuff

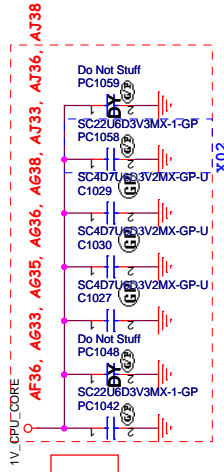


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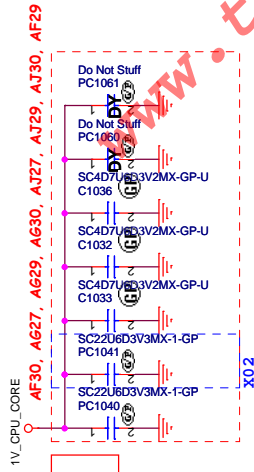
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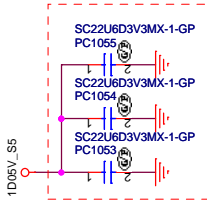
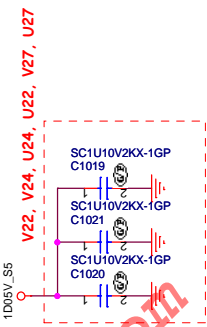
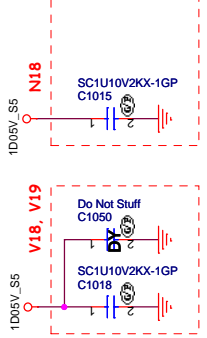
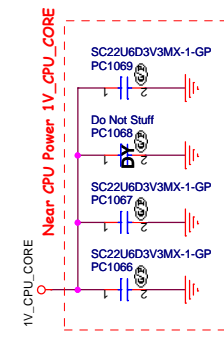
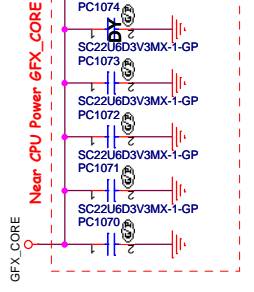
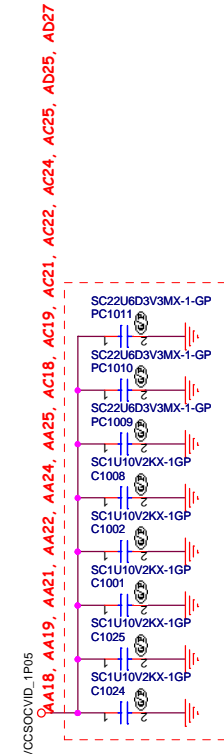
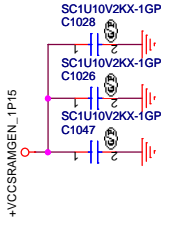
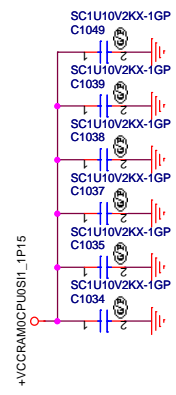
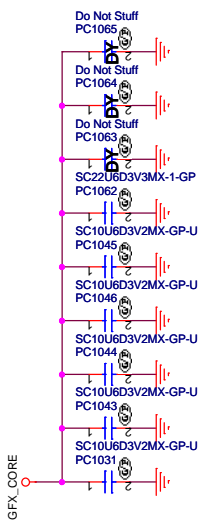
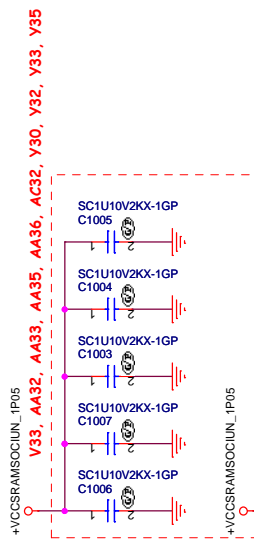
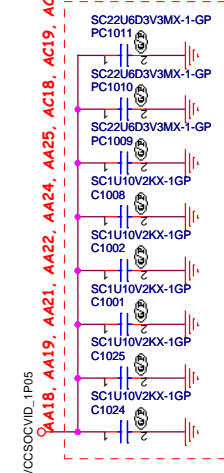
SSID = CPU



PLACE ALL THE CAPS
UNDER THE PKG SHADOW



PLACE ALL THE CAPS
UNDER THE PKG SHADOW



PLACE CLOSE TO PIN 1 OF RB

PLACE CLOSE TO PIN 1 OF RA

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File: CPU (Power CAP1)

Size: A3

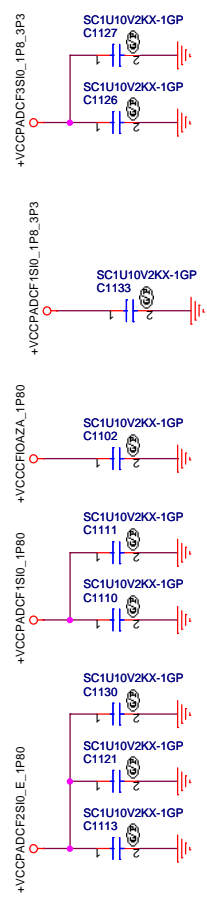
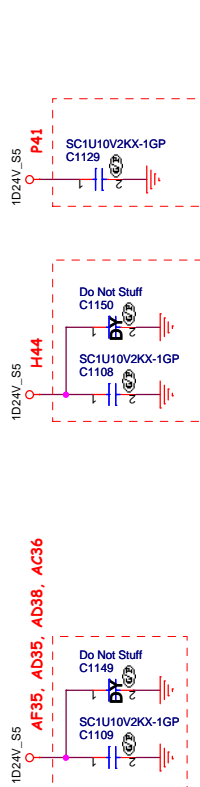
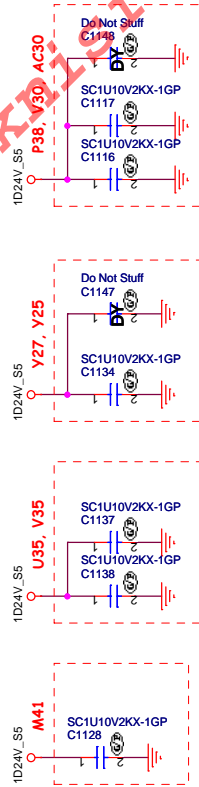
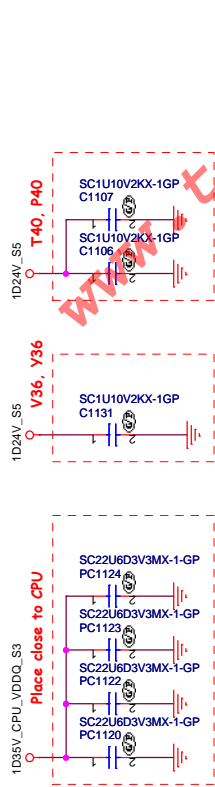
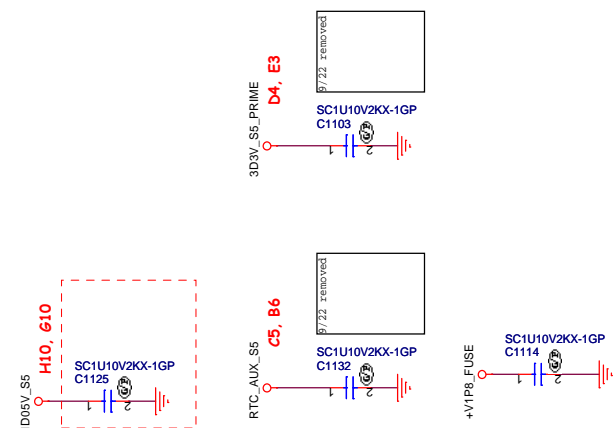
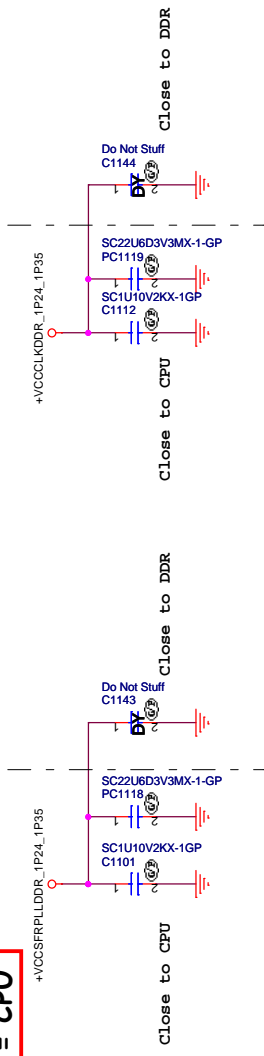
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Rev: 103

Sheet: 10 of 103

SSID = CPU



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SSID = MEMORY

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Date: Thursday, March 19, 2015		Sheet 13 of	109


SSID = CPU

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Size A4	Document Number Redwood BSW 11.6"		Rev A00
Date: Thursday, March 19, 2015		Sheet 14 of	109

SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

All the straps are sampled on the rising edge of the
PMC_RSMRST_N signal (check list)

Description	DDI0_Detected	DDI1_Detected	A16 Swap Override	DSI Display Detected	Boot BIOS Strap BBS	Flash Descriptor Security Override	DFX Boot Halt Strap & VISA Early POSM Debug Enable	DFX Sus Debug Strap	ICLK, USB2, DDI SFR Supply Select	ICLK SFR Bypass	POSM Select	ICLK Xtal OSC Bypass	CCU SUS RO Bypass	RTC OSC bypass
GPIO	GPIO_SUS0	GPIO_SUS1	GPIO_SUS2	GPIO_SUS3	GPIO_SUS4	GPIO_SUS5	GPIO_SUS6	GPIO_SUS7	SEC_GPIO_SUS8	SEC_GPIO_SUS9	SEC_GPIO_SUS10	GP_CAMERASB08	GP_CAMERASB09	GP_CAMERASB11
Schematic														
High	DDI0 Detect	DDI1 Detect	Normal Operation	DSI Detect	Boot from SPI	Weak internal pull-up Normal Operation	Normal	Weak internal pull-up Normal	1.35V	Weak internal pull-up Bypass with 1.05V	PMC	Bypass	Bypass	Bypass
Low	Disable	Disable	Change Boot Loader address (A16 Override)	Disable	Boot from LPC	Override	Halt boot enable	Sus Debug enable	1.25V	No bypass	Fuse controller	No bypass	No bypass	No bypass

Table 29. Straps (Sheet 1 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDI0 Detect	Weak internal pull-down	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	DDI1 Detect	Weak internal pull-down	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	A16 swap override	Weak internal pull-up	Top Swap (A16 Override) 0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[4]	Boot BIOS Strap BBS	Weak internal pull-up	BIOS Boot Selection 0 = - 1 = SPI
GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal pull-up	Security Flash Descriptors 0 = Override 1 = Normal Operation

Table 29. Straps (Sheet 2 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[8]	ICLK, USB2, DDI SFR Supply Select	Weak internal pull-down	0 = Supply is 1.25V 1 = Supply is 1.35V This strap also contains PLL LDO 0: supply is 1.25V; 1: supply is 1.35V. Selects supply voltage for LDOs used for PLLs, thermal oscillators, USB2, ICLK and DDI
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal pull-up	0 = No bypass 1 = Bypass with 1.05V
GPIO_SUS[10]	POSM Select	Weak internal pull-down	Selects which POSM will be observed at time 0 0 = Fuse controller 1 = PMC
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass


CHV Straps [CRB] -- strap detect @ RSMRST# assertion				
Purpose	CHV Pin Name (refer CHV symbol PIN)	PU/PD (internal - Weak)	Options	Default State on board?
DDI0 Detected	GPIO_SUS0	PD	1- DDI0 Detect, 0- Disable	High
DDI1 Detected	GPIO_SUS1	PD	1- DDI1 Detect, 0- Disable	High
A16 swap override	GPIO_SUS2	PU	1- Default, 0- A16 override	High
DSI Display Detected	GPIO_SUS3	PD	1- DSI detect, 0- Disable	Low
Boot BIOS Strap BBS	GPIO_SUS4	PU	1- Boot from SPI, 0- Boot from LPC	High
Flash Descriptor Security Override	GPIO_SUS5	PU	1- Security enabled, 0- Security disabled	High
DFX Boot Halt Strap & VISA Early POSM Debug Enable	GPIO_SUS6	PU	1- normal, 0- Halt boot enable	High
DFX Sus Debug Strap	GPIO_SUS7	PU	1- Normal, 0- Sus Debug enable	High
ICLK, USB2, DDI SFR Supply Select	SEC_GPIO_SUS8	PU	1- 1.35V, 0- 1.25V	Low
ICLK SFR Bypass	SEC_GPIO_SUS9	PD	1- Bypass with 1.05V, 0- No Bypass	Low
POSM Select	SEC_GPIO_SUS10	PD	1- PMC, 0- Fuse controller	Don't care, if GPIO_SUS6 is pulled high.
ICLK Xtal OSC Bypass	GP_CAMERASB08	PD	1- Bypass, 0- No bypass	Low
CCU SUS RO Bypass	GP_CAMERASB09	PD	1- Bypass, 0- No bypass	Low
RTC OSC Bypass	GP_CAMERASB11	PD	1- Bypass, 0- No bypass	Low

SSID = CPU

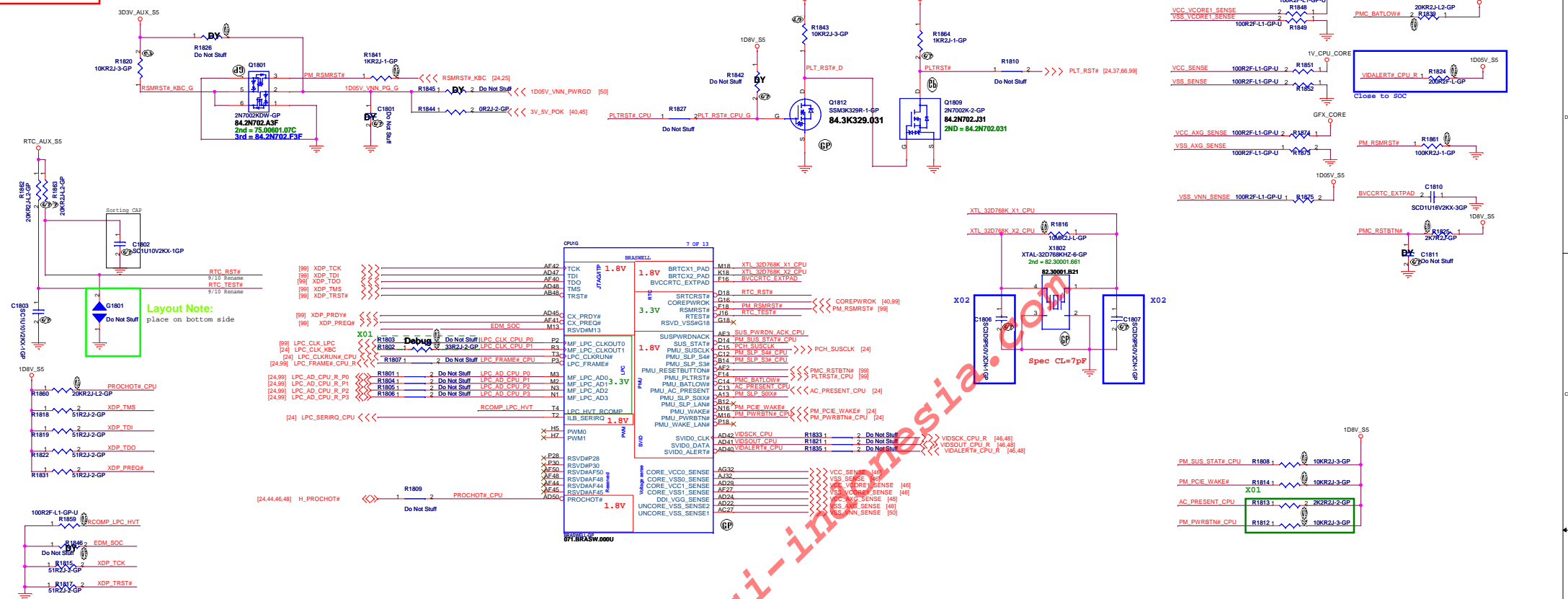
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Date: Thursday, March 19, 2015		Sheet 17 of	109

SSID = PCH



APS debug port

Do Not Stuff	TP1801	1	PM_SLP_S3#
Do Not Stuff <td>TP1802<td>1<th>PM_SLP_S4#</th></td></td>	TP1802 <td>1<th>PM_SLP_S4#</th></td>	1 <th>PM_SLP_S4#</th>	PM_SLP_S4#
Do Not Stuff <td>TP1803<td>1<th>RTC_RST#</th></td></td>	TP1803 <td>1<th>RTC_RST#</th></td>	1 <th>RTC_RST#</th>	RTC_RST#
Do Not Stuff <td>TP1804<td>1<td></td></td></td>	TP1804 <td>1<td></td></td>	1 <td></td>	
Do Not Stuff <td>TP1805<td>1<th>APS_PMC_RSTB#</th></td></td>	TP1805 <td>1<th>APS_PMC_RSTB#</th></td>	1 <th>APS_PMC_RSTB#</th>	APS_PMC_RSTB#
Do Not Stuff <td>TP1806<td>1<th>APS_SLP_S00X#</th></td></td>	TP1806 <td>1<th>APS_SLP_S00X#</th></td>	1 <th>APS_SLP_S00X#</th>	APS_SLP_S00X#

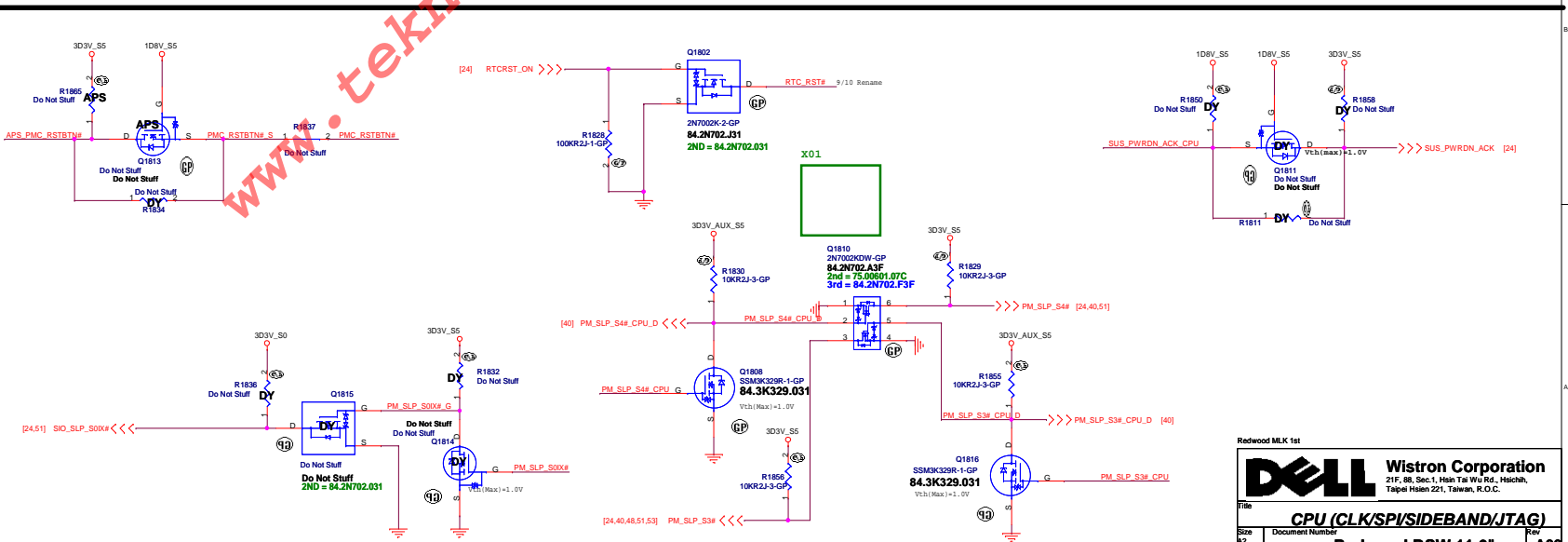
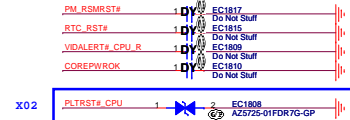
Handwritten notes on the diagram:

- Red double arrows pointing to TP1804: KBC_PWRBRTN# [24.66.99]
- Red double arrows pointing to TP1806: Do Not Stuff
- Red double arrows pointing to TP1806: SIO_SLP_S00X#
- Red double arrows pointing to TP1806: **DO NOT STUFF**

reserve the 0402 0.1u caps on reset for EMI.



reserve the 0402 0.1u caps on reset for EMI

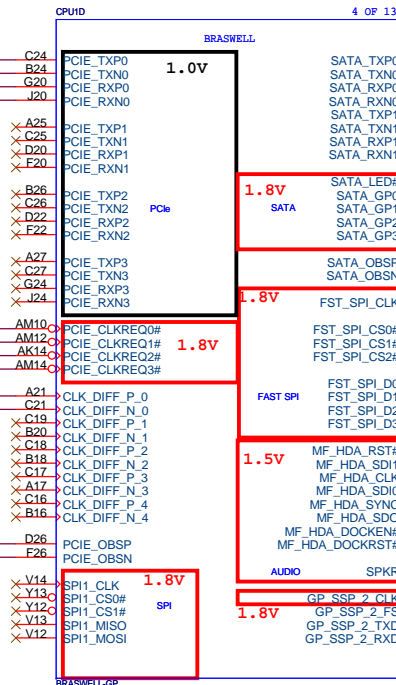


SSID = PCH

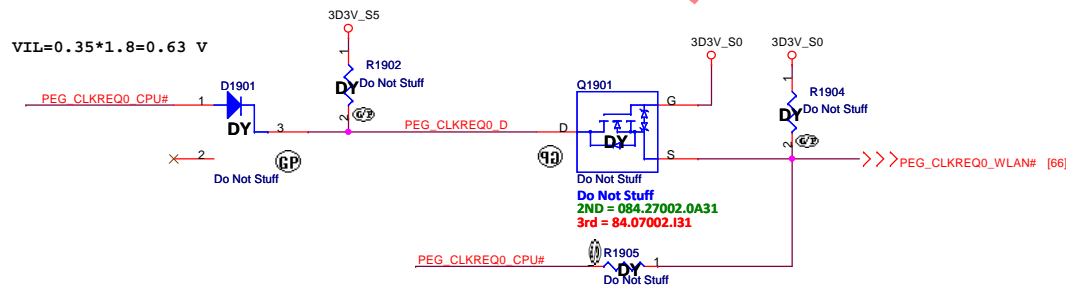
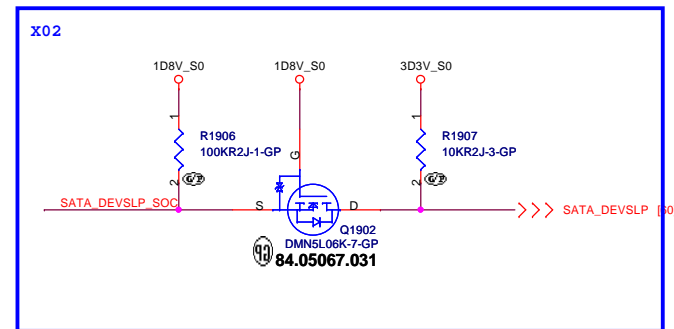
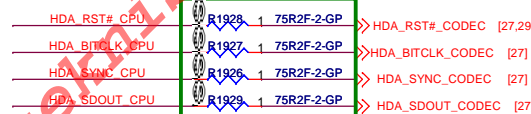
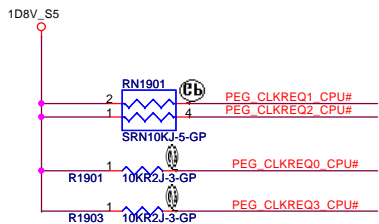
WLAN

[66] PCIE_TX_CON_P0
[66] PCIE_TX_CON_N0
[66] PCIE_RX_CPU_P0
[66] PCIE_RX_CPU_N0

C1915 2 1 SCD1U16V2KX-3GP PCIE_TX_CPU_P0 C24
C1916 2 1 SCD1U16V2KX-3GP PCIE_TX_CPU_N0 B24
G20
J20



HDD



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SSID = PCH

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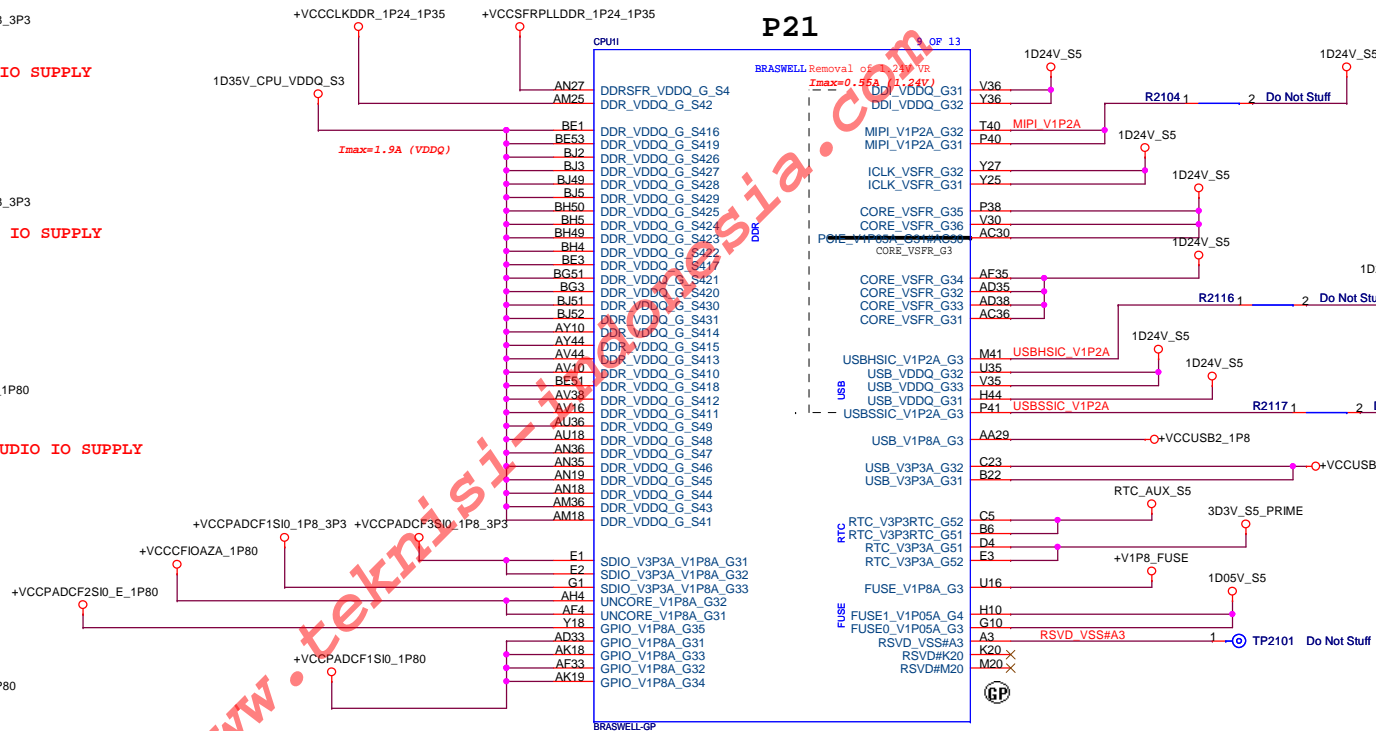
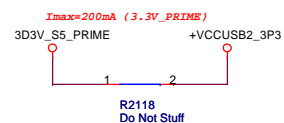
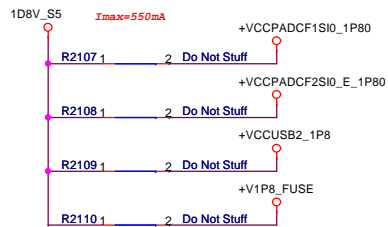
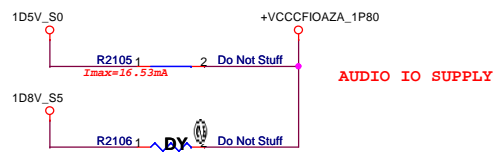
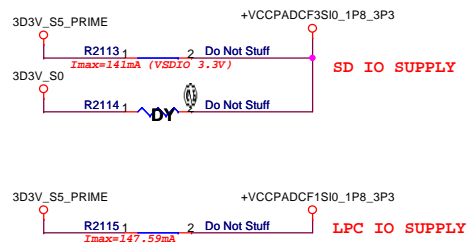
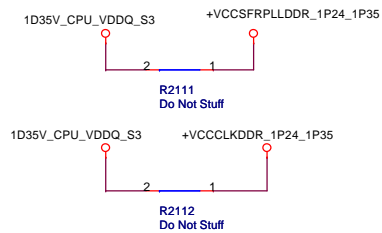
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Title																													

CPU (POWER1)Size
A3

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Sheet 21 of 109

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Sheet 22 of 109

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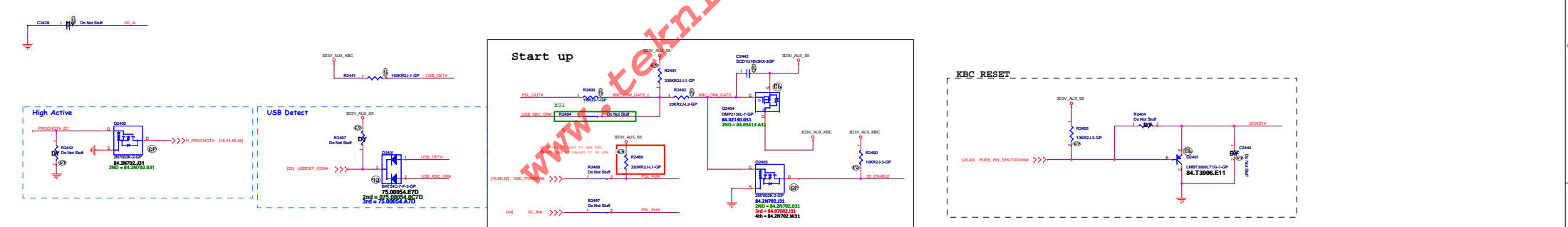
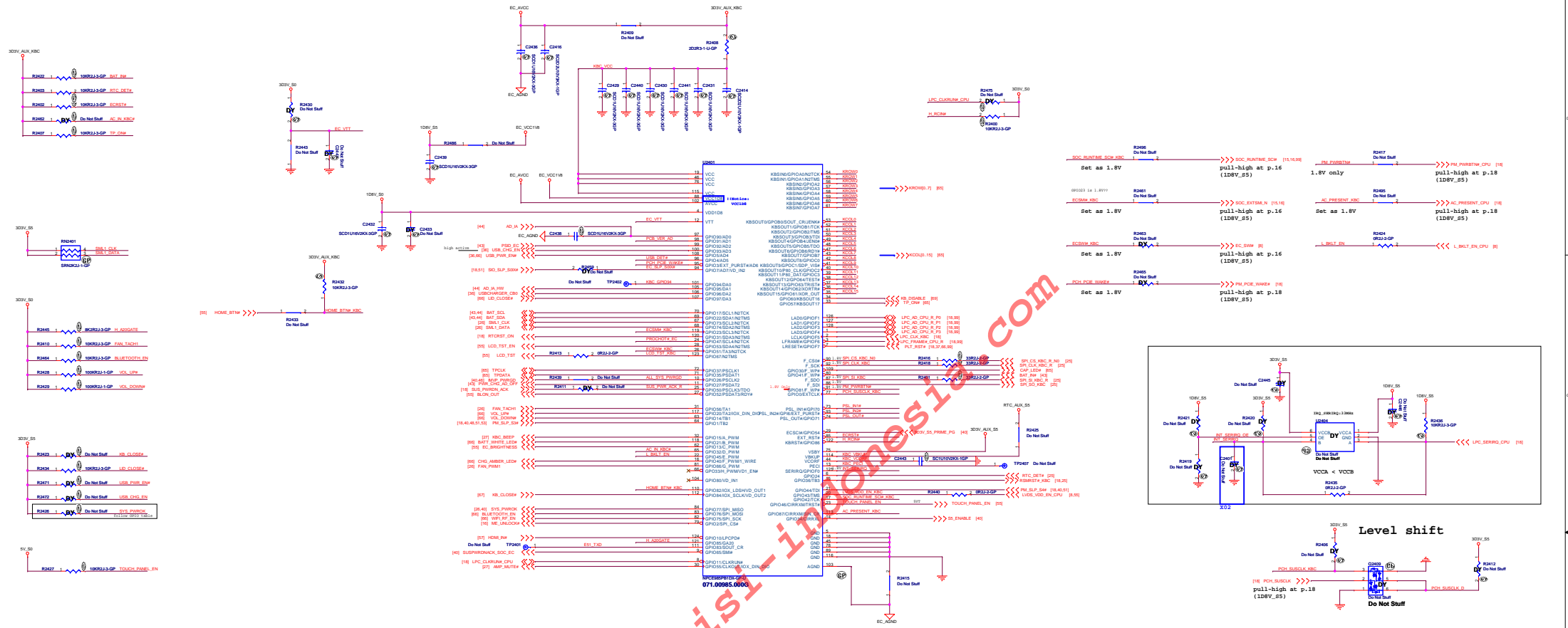
Rev

A00

Date: Thursday, March 19, 2015

Sheet 23 of 109

SSID = KBC



FMT Request									
AVS_PWDN	DV-1	EC2459	Do Not Stuff						
BLUETOOTH_EN	DV-1	EC2459	Do Not Stuff						
WIFI_RF_EN	DV-1	EC2459	Do Not Stuff						
SL_ENABLE	DV-1	EC2459	Do Not Stuff						

Start up									
PSL_OUT2	X01	EC2459	Do Not Stuff						
USB_HNC_CSN	F-RS44	EC2459	Do Not Stuff						
USB_HNC_CSN	F-RS44	EC2459	Do Not Stuff						
AC_INW	TP2401	EC2459	Do Not Stuff						

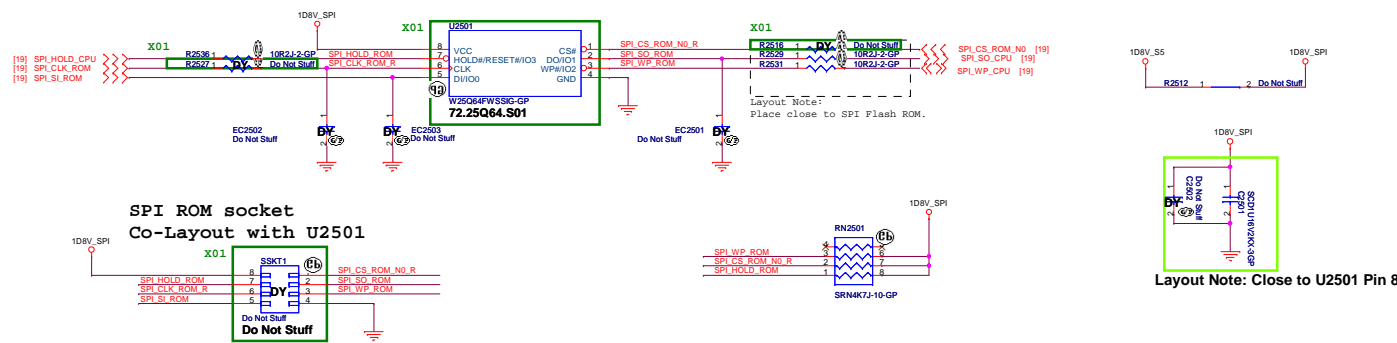
KBC_RESET									
PURE_HV_SHUTDOWN		EC2459	Do Not Stuff						

Level shift									
PCH_SUSCLK_KBC		EC2459	Do Not Stuff						
PCH_SUSCLK_D		EC2459	Do Not Stuff						

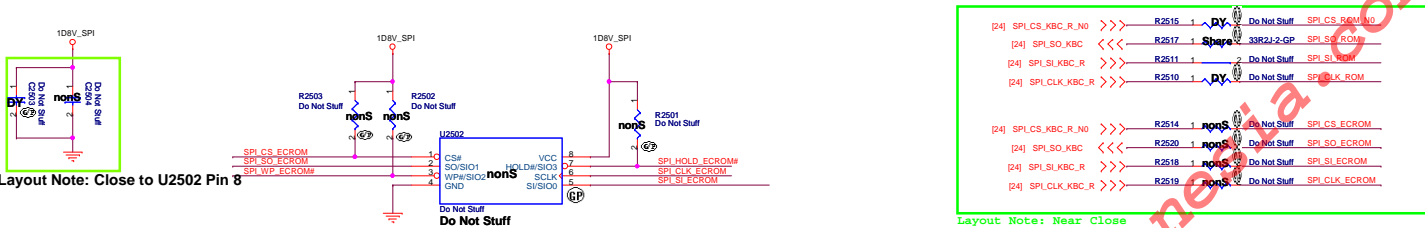
EC - MECS085									
SA	100.0 K	10.0 K	3.000 V	3.0054	2.9945	>= 2.975 V			
SB	100.0 K	20.0 K	2.750 V	2.7591	2.7409	>= 2.616 V	< 2.875 V		
SC	100.0 K	33.0 K	2.481 V	2.4935	2.4688	>= 2.363 V	< 2.616 V		
-1	100.0 K	47.0 K	2.245 V	2.2592	2.2305	>= 2.123 V	< 2.363 V		
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169	1.9854	>= 1.894 V	< 2.123 V		
Reserved for project use	100.0 K	76.8 K	1.887 V	1.8933	1.7559	>= 1.758 V	< 1.834 V		
Reserved for project use	100.0 K	100.0 K	1.850 V	1.8635	1.6035	>= 1.504 V	< 1.750 V		
Reserved for project use	100.0 K	143.0 K	1.350 V	1.3740	1.3421	>= 1.281 V	< 1.594 V		
Reserved for project use	100.0 K	174.0 K	1.284 V	1.2197	1.1891	>= 1.126 V	< 1.381 V		
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	1.0234	>= 0.924 V	< 1.126 V		

SSID = Flash.ROM

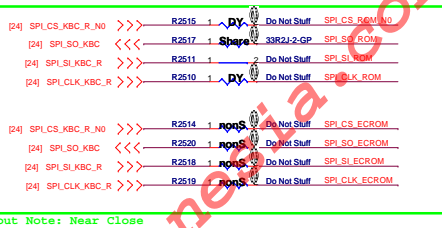
SPI FLASH ROM (8M byte) for CPU



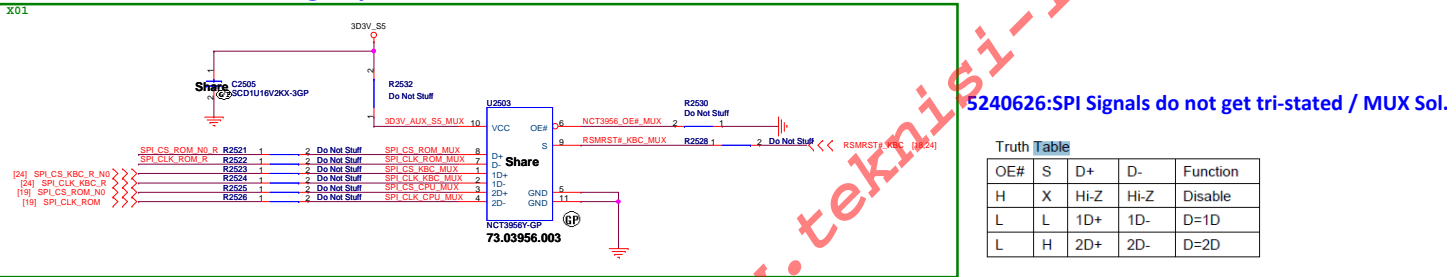
SPI FLASH ROM (128k byte) for KBC



SPI ROM link to KBC



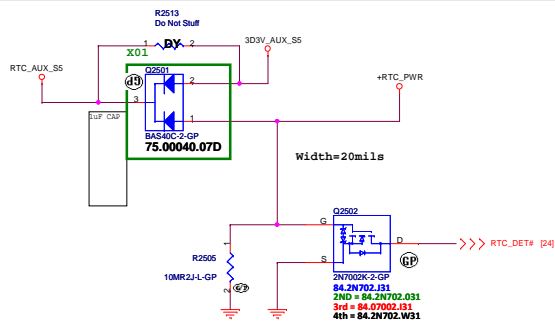
High Speed Switch for Share ROM



5240626:SPI Signals do not get tri-stated / MUX Sol.

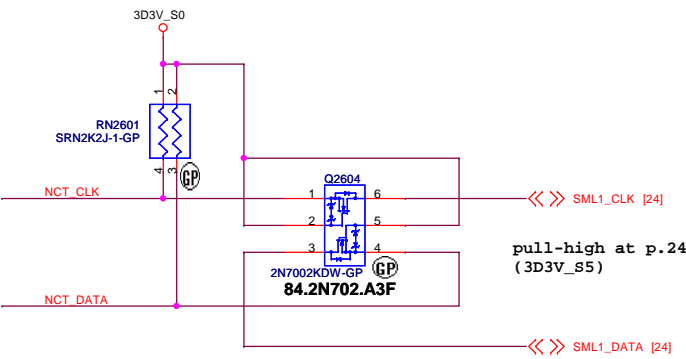
OE#	S	D+	D-	Function
H	X	Hi-Z	Hi-Z	Disable
L	L	1D+	1D-	D=1D
L	H	2D+	2D-	D=2D

SSID = RTC

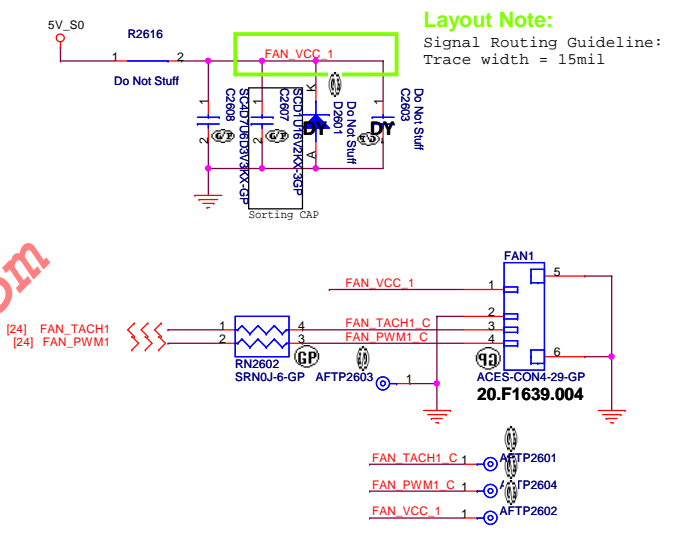


SSID = Thermal

- EE Note:
- 1. T8: PURE_HW_SHUTDOWN# through Q2603.
 - 2. THM_SENSOR: Thermal sensor NCT7718W solution.

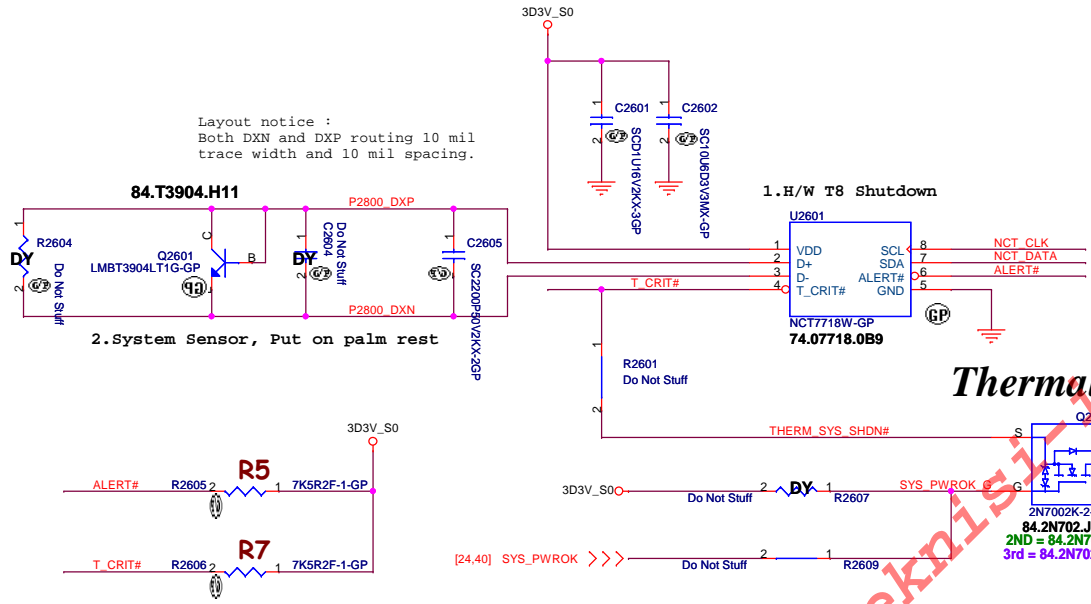


PWM FAN1



Layout Note:
Signal Routing Guideline:
Trace width = 15mil

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.

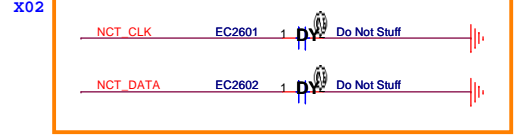


Thermal sensor NCT 7718W

The default value is trapping after power up 100ms by different pull-up resistors of T_CRIT# and ALERT# pin:

TEMPERATURE (°C)	T_CRIT#				
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107
	7.5KΩ	79	89	99	109
	10.5KΩ	81	91	101	111
	14KΩ	83	93	103	113
	18.7KΩ	85	95	105	115

Layout Note: Close U2601



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Title

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Size
A4

Document Number

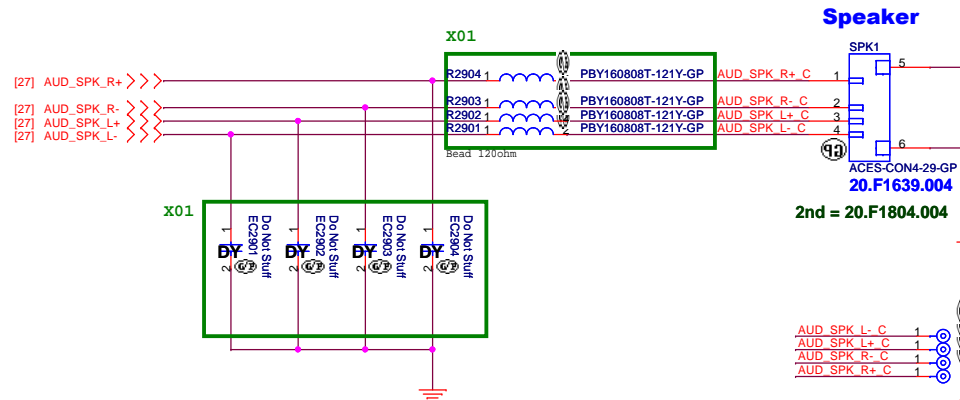
Redwood BSW 11.6"

Rev
A00

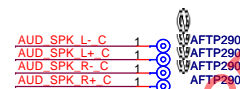
Date: Thursday, March 19, 2015

Sheet 28 of 109

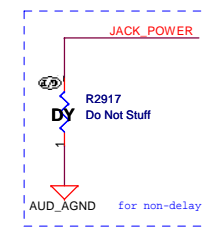
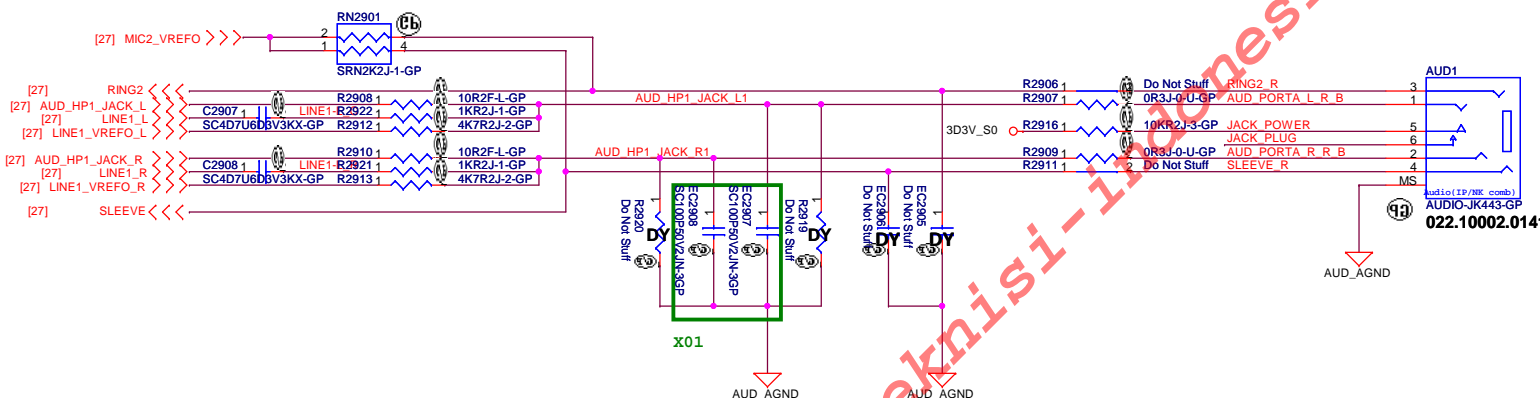
SSID = AUDIO



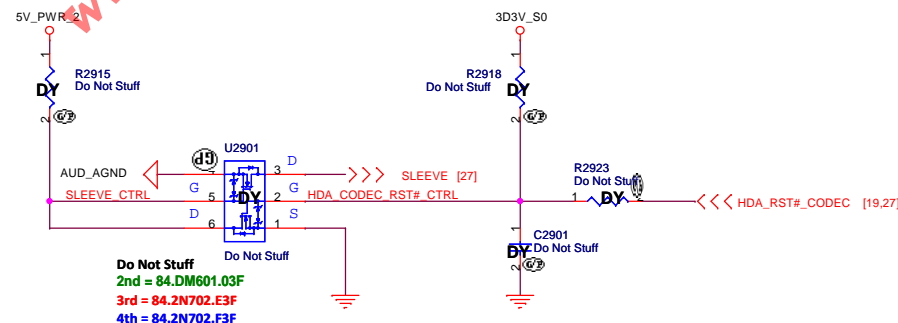
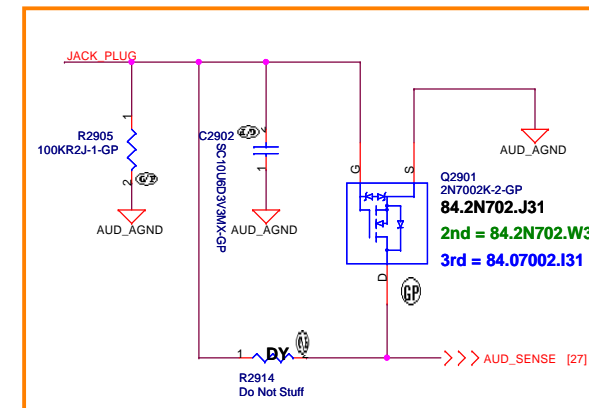
CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-



Combo Jack



Delay circuit



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Title			Speaker/HPMIC CONN
Size	Document Number	Rev	
A3	Redwood BSW 11.6"	A00	
Date:	Thursday, March 26, 2015	Sheet	29 of 109

SSID = LOM

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Title

(Reserved)LOM

Size
A4

Document Number

Redwood BSW 11.6"

Rev
A00

Date: Thursday, March 19, 2015


Sheet 30 of 109

SSID = LAN

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Title (Reserved)LAN					
Size A4		Document Number Redwood BSW 11.6"			Rev A00
Date: Thursday, March 19, 2015			Sheet 31 of 109		

SSID = LAN CONN

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Title (Reserved)RJ45+Transformer		
Size A4	Document Number Redwood BSW 11.6"	Rev A00
Date: Thursday, March 19, 2015		Sheet 32 of 109

SSID = Card Reader

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Title

(Reserved)Card Reader + CONN

Size
A4

Document Number

Redwood BSW 11.6"

Rev
A00

Date: Thursday, March 19, 2015

Sheet 33 of 109

SSID = USB

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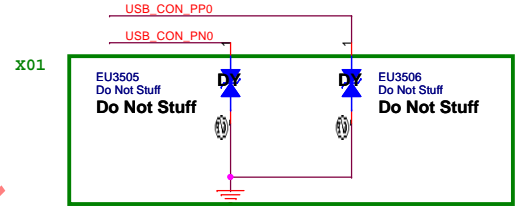
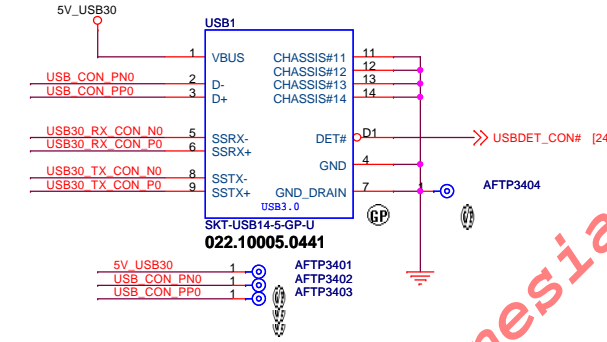
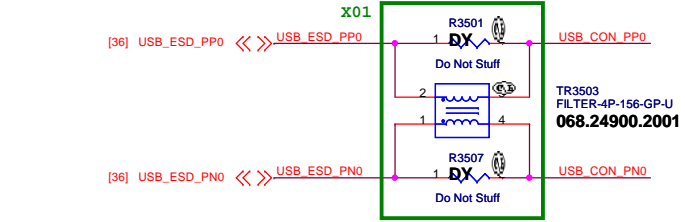
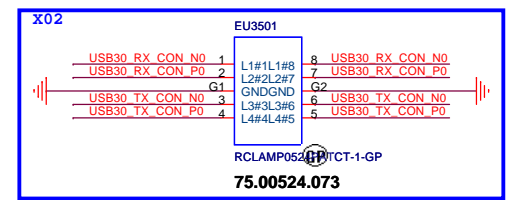
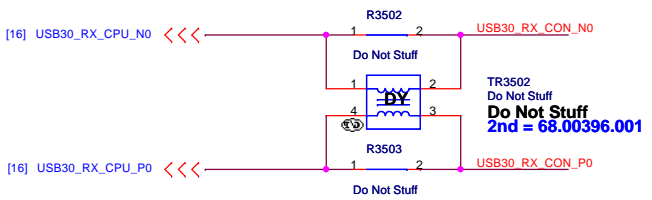
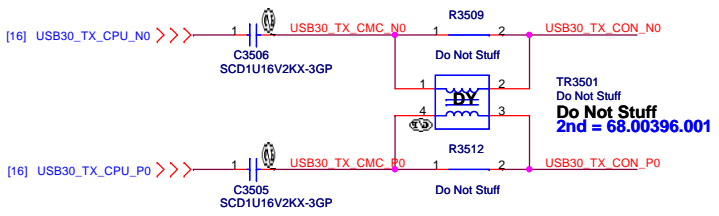
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Title
(Reserved)USB 2.0 Port

Size A4	Document Number Redwood BSW 11.6"	Rev A00
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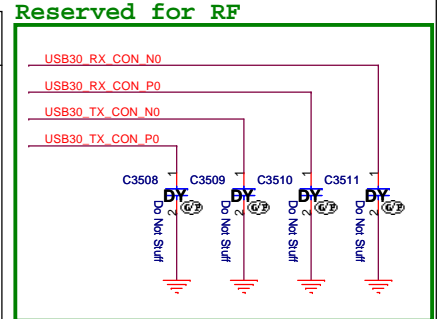
Date: Thursday, March 19, 2015 Sheet 34 of 109

SSID = USB

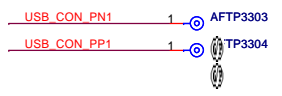
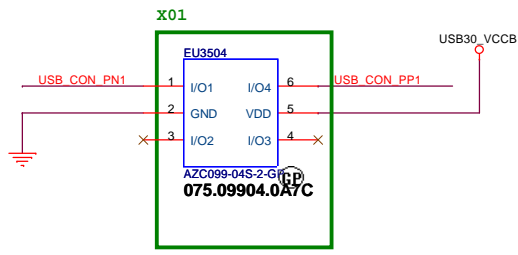
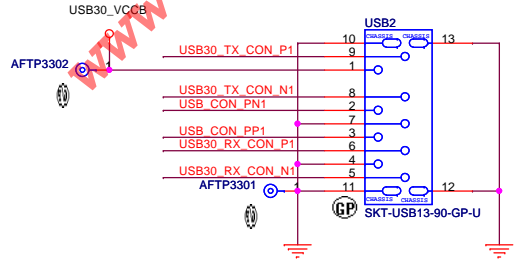
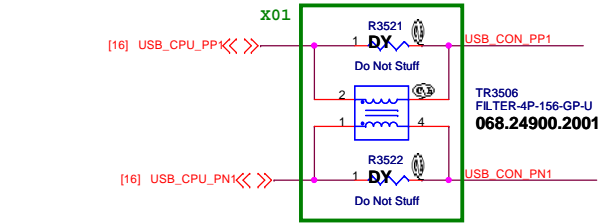
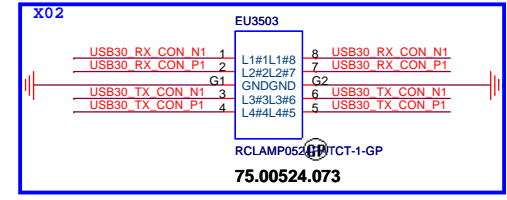
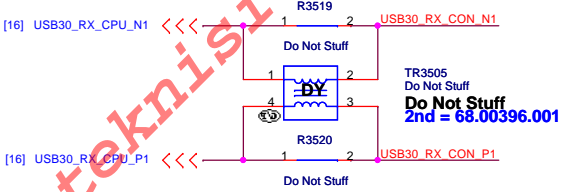
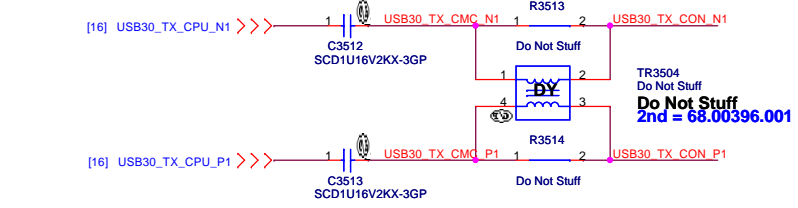


USB 3.0 Connector
Pin definition

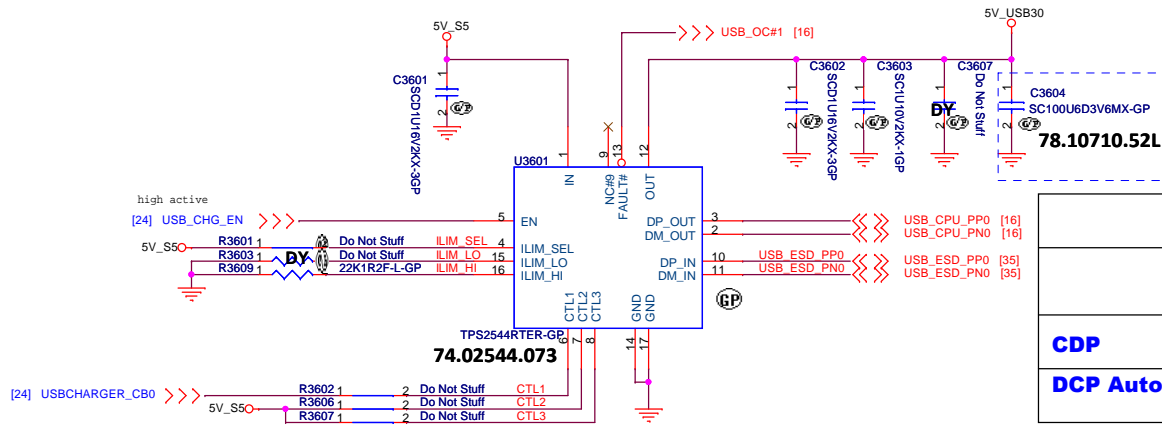
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+ SuperSpeed RX
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+ SuperSpeed TX



USB3.0 Port2



USB Charger Port1

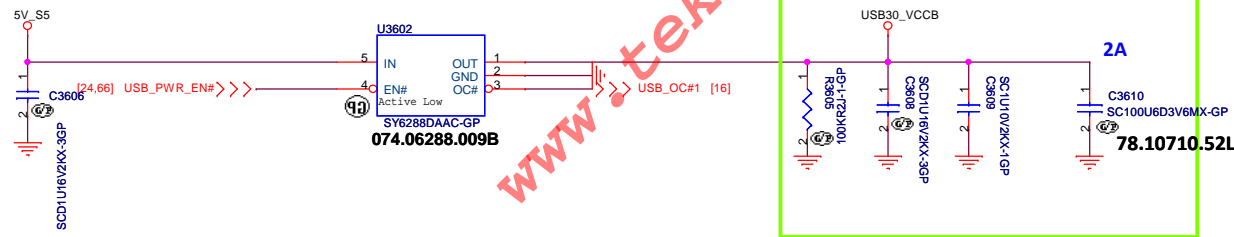


If MLCC is used as Main Source.
Inform Layout team to remark Pin 1 as positive.
In case MLCC shortage and other type of Cap With Polarity Is Used.

Device Control Pins

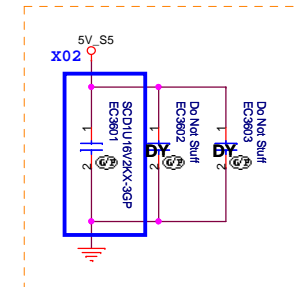
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

USB3.0 Port2



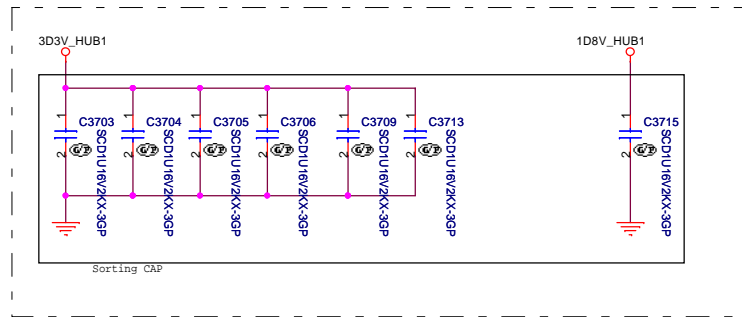
Layout Note: Close CON1

Reserved For Antenna

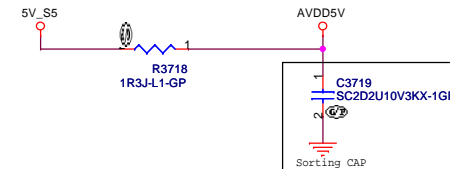
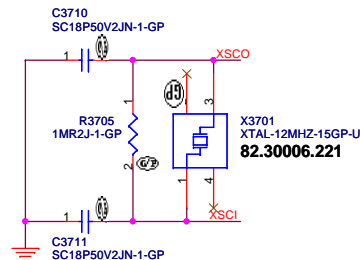
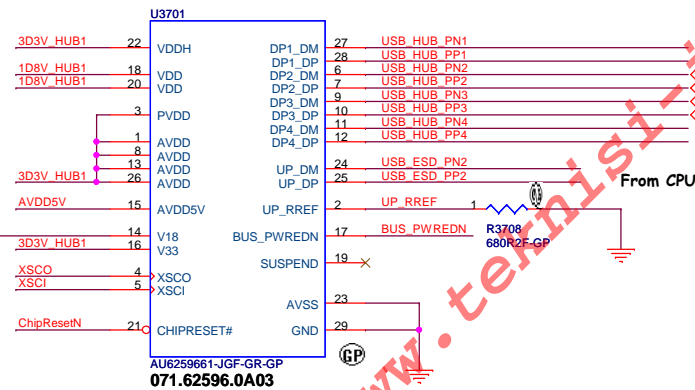
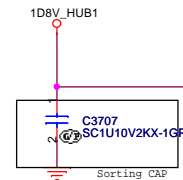
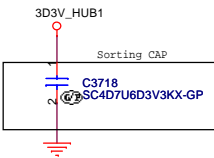
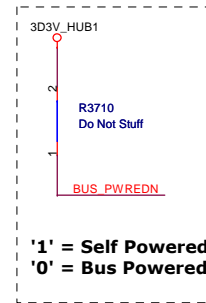


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SSID = USB



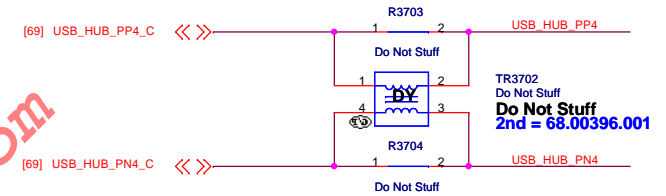
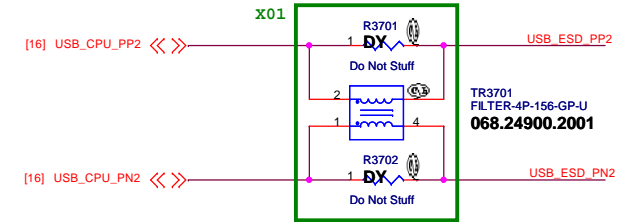
Near the chip side.



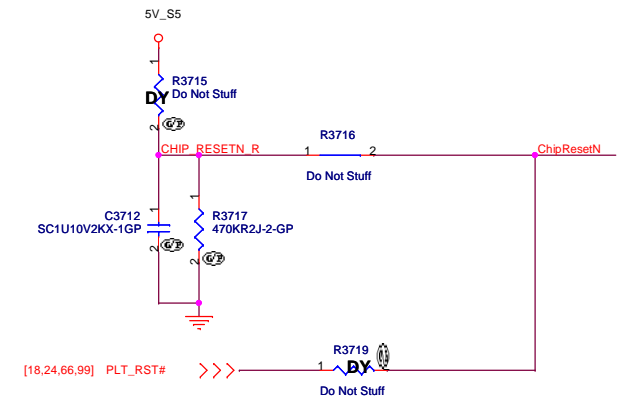
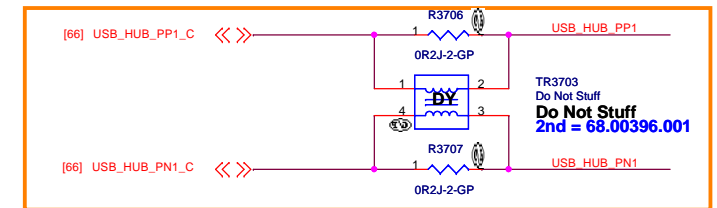
USB2.0 Port3
Card Reader
Bluetooth
Sensor Hub

USB Table

Pair	Device
1	USB2.0 Port3
2	Card Reader
3	Bluetooth
4	Sensor Hub



A00 Layout Note: Need Close CONN IOBD1



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Title: **USB2.0 HUB**

Size: A3 Document Number: **Redwood BSW 11.6"** Rev: **A00**

Date: Wednesday, March 25, 2015 Sheet: 37 of 109

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Size
A4

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Rev
A00

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Sheet 38 of 109

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Rev

A00

Date: Thursday, March 19, 2015

Sheet 41 of 109

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Document Number

Redwood BSW 11.6"

Rev
A00

Date: Thursday, March 19, 2015

Sheet 42 of 109

```
SSID = PWR.Support
```

ndde close to EL4202

PSID Layout width > 25mil

2nd = 20.F1804.006

EMI requirement

3rd = 84.07002.I31
2nd = 84.2N702.W
84.2N702.J31

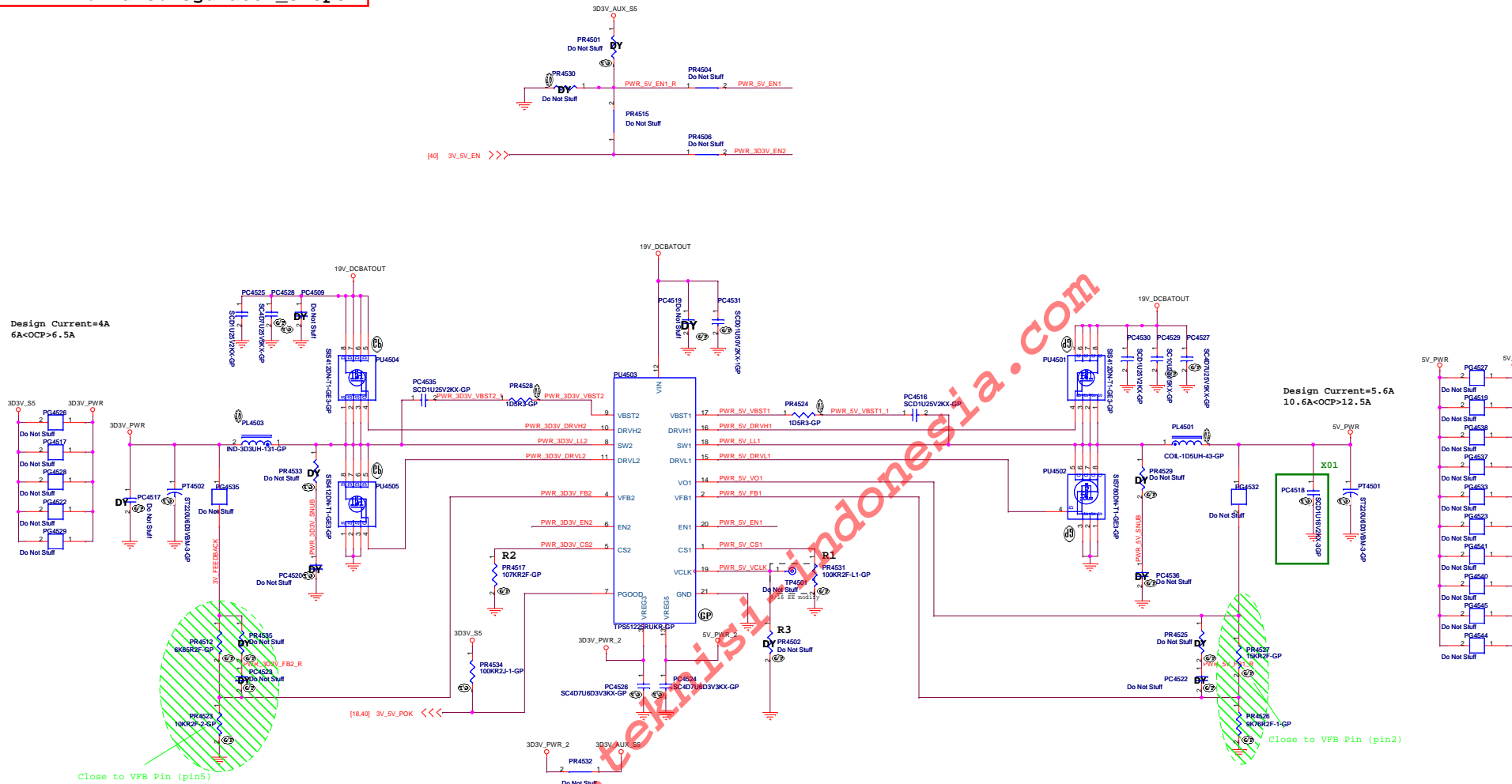
[24] PWR_CHG_AD_OFF >>> PR4312
1KR2J-1-GP

EMI requirement

SSID = PWR.Plane.Regulator_5v3p3v

Design Current=4A
6A<OCP>6.5A

Design Current=5.6A
10.6A<OCP>12.5A



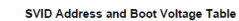
I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKER 4.7UH PCMB063T-4R7MS Cynotec 28mohm/33mohm Isat =6.5Arms 68.4R71A.20H
O/P cap:CHIP CAP T 220U 6.3V M3528 PSL /NEC/ 25mOhm / 77.C2271.45L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKER 2.2UH PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap:CHIP CAP T 220U 6.3V M3528 PSL /NEC/ 25mOhm / 77.C2271.45L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

TPS51225 & TPS51285 Co-Lay

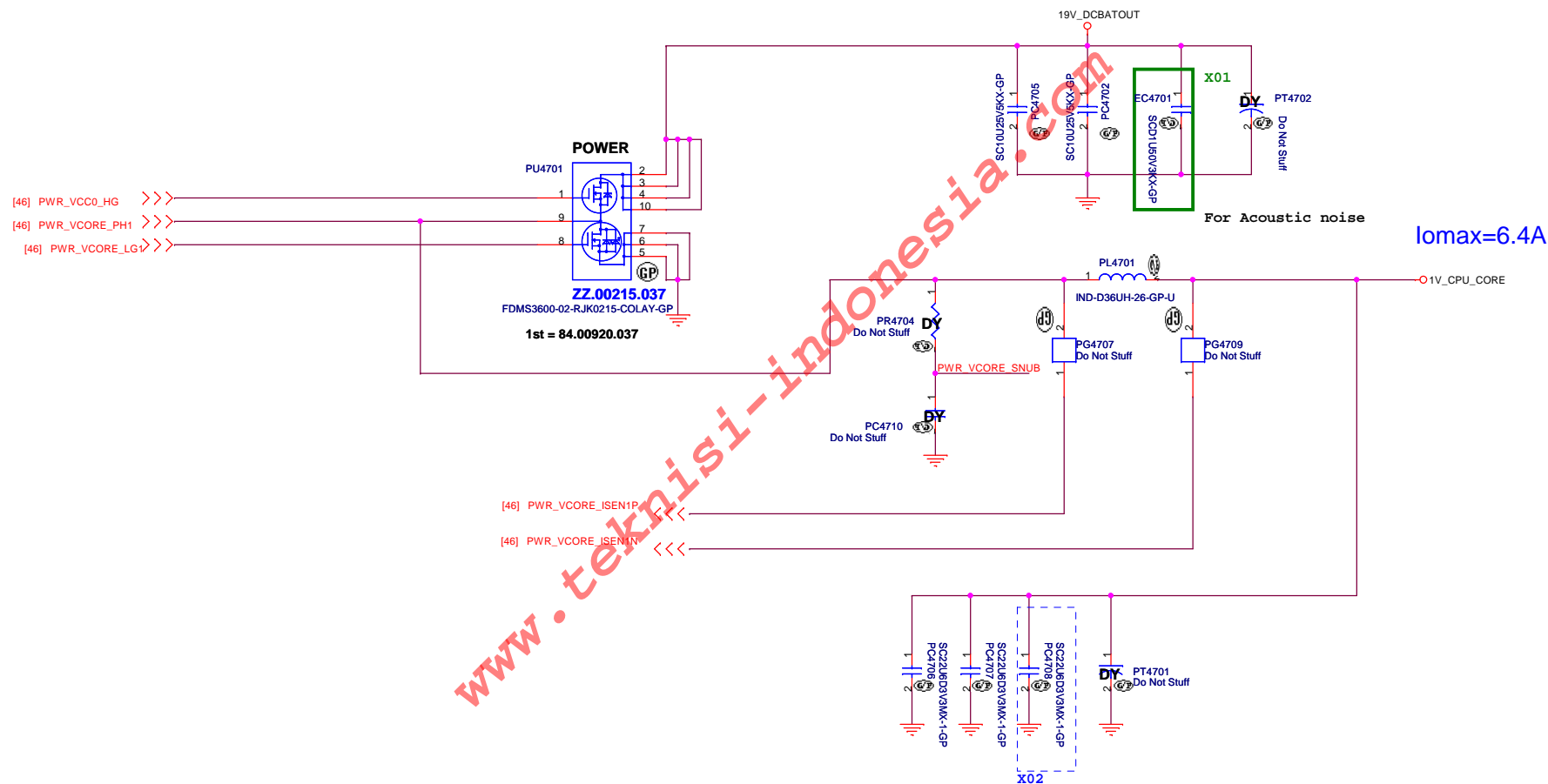
	TPS51225	TPS51285
R1	100K	20K
R2	107K	21.5K
R3	DY	200

Redwood MLK 1st



VBOOT/ADDR Resistor (Ohm)	SVID Address	Vboot (V)
0	0x0	1.0
14.0 k	0x1	1.0
22.1 k	0x2	1.0
30.1 k	0x3	1.0
39.2 k	0x4	1.0
48.7 k	0x5	1.0
57.6 k	0x6	1.0
68.1 k	0x7	1.0
78.7 k	0x8	1.1
88.7 k	0x9	1.1
100 k	0x1	1.1
113 k	0x2	1.1
124 k	0x3	1.1
137 k	0x4	1.1
150 k	0x5	1.1
165 k	0x6	1.1
178 k	0x7	1.1
196 k	0x8	1.1

SSID = CPU Regulator



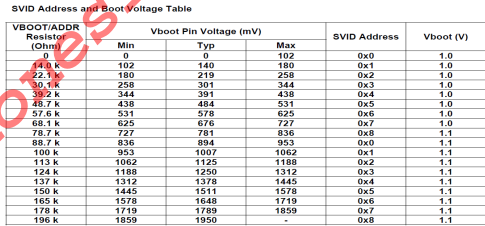
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Title		NCP81201MNTXG CPUCORE(2/3)	
Size	Document Number	Rev	
A3			A00
Date:	Wednesday, March 25, 2015	Sheet	47 of 109


SSID = GFX Regulator



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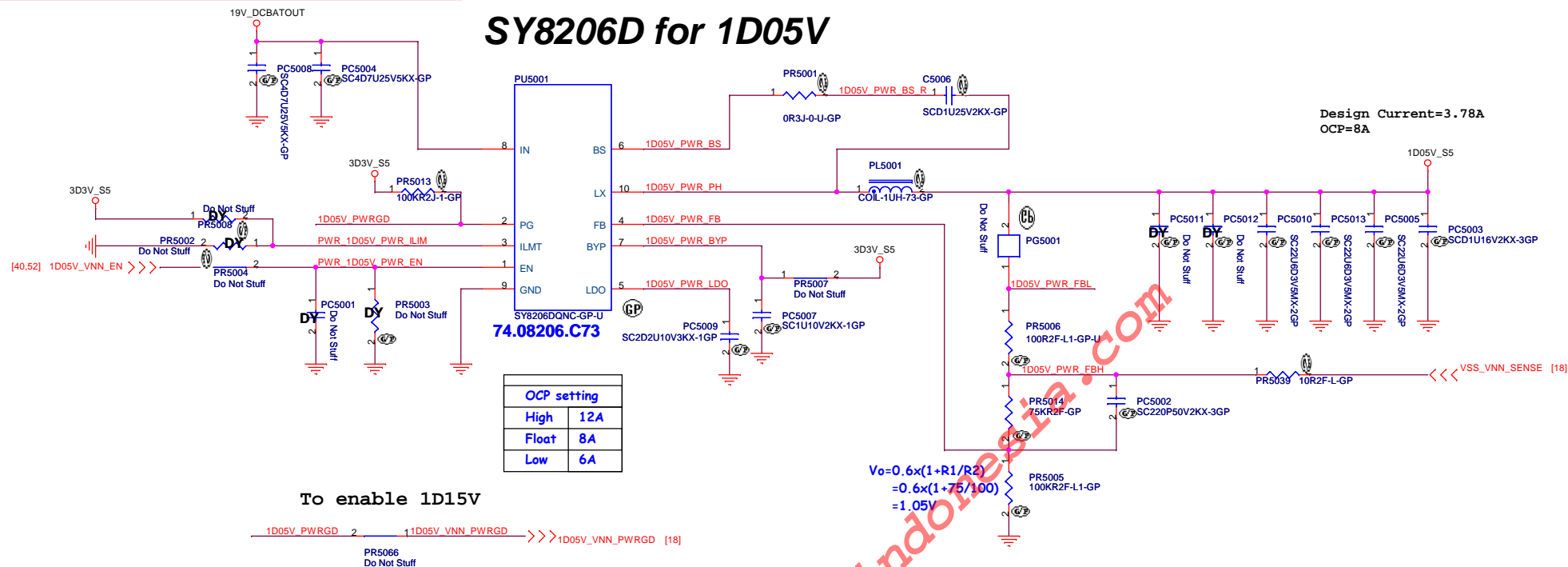
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Title (Reserved)			
Size A4	Document Number Redwood BSW 11.6"		Rev A00
Date: Thursday, March 19, 2015		Sheet 49 of	109

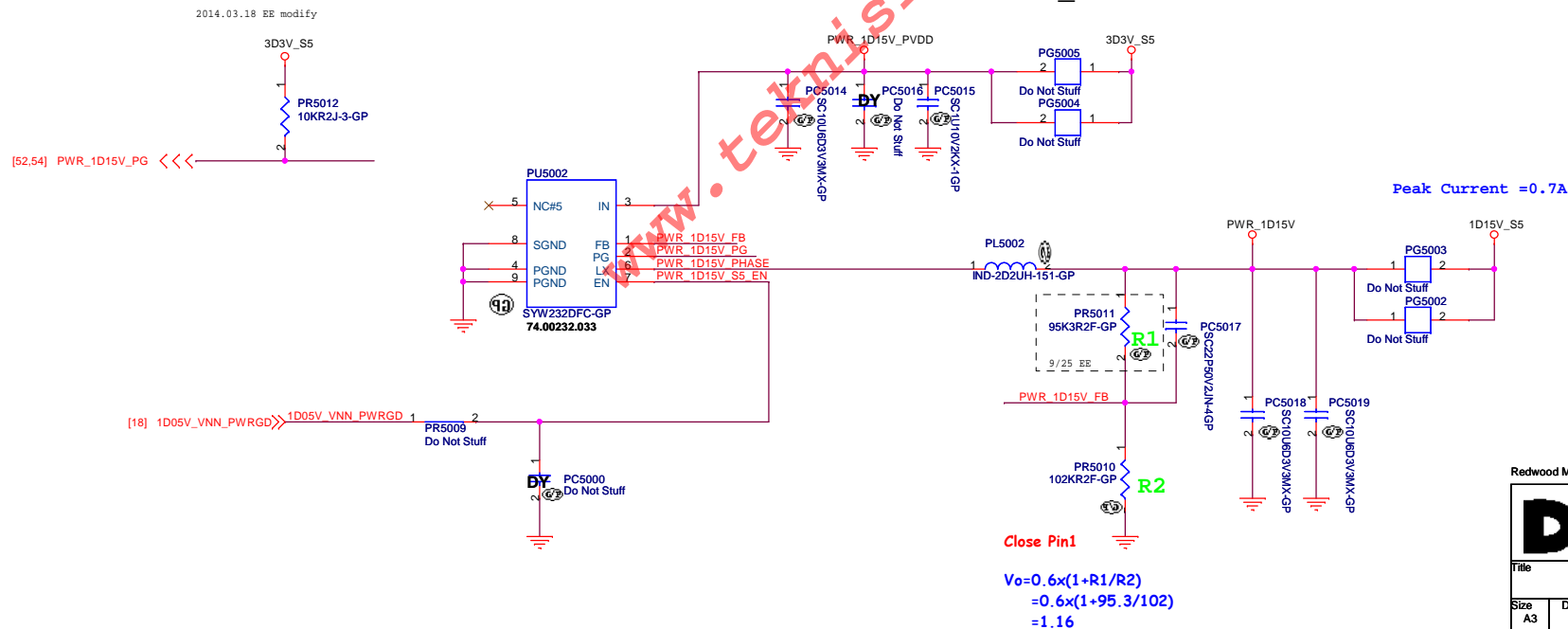
SSID = PWR.Plane.Regulator_1p05v

SY8206D for 1D05V



SSID = PWR.Plane.Regulator_1p8v

SYW232 for 1D15V_S5



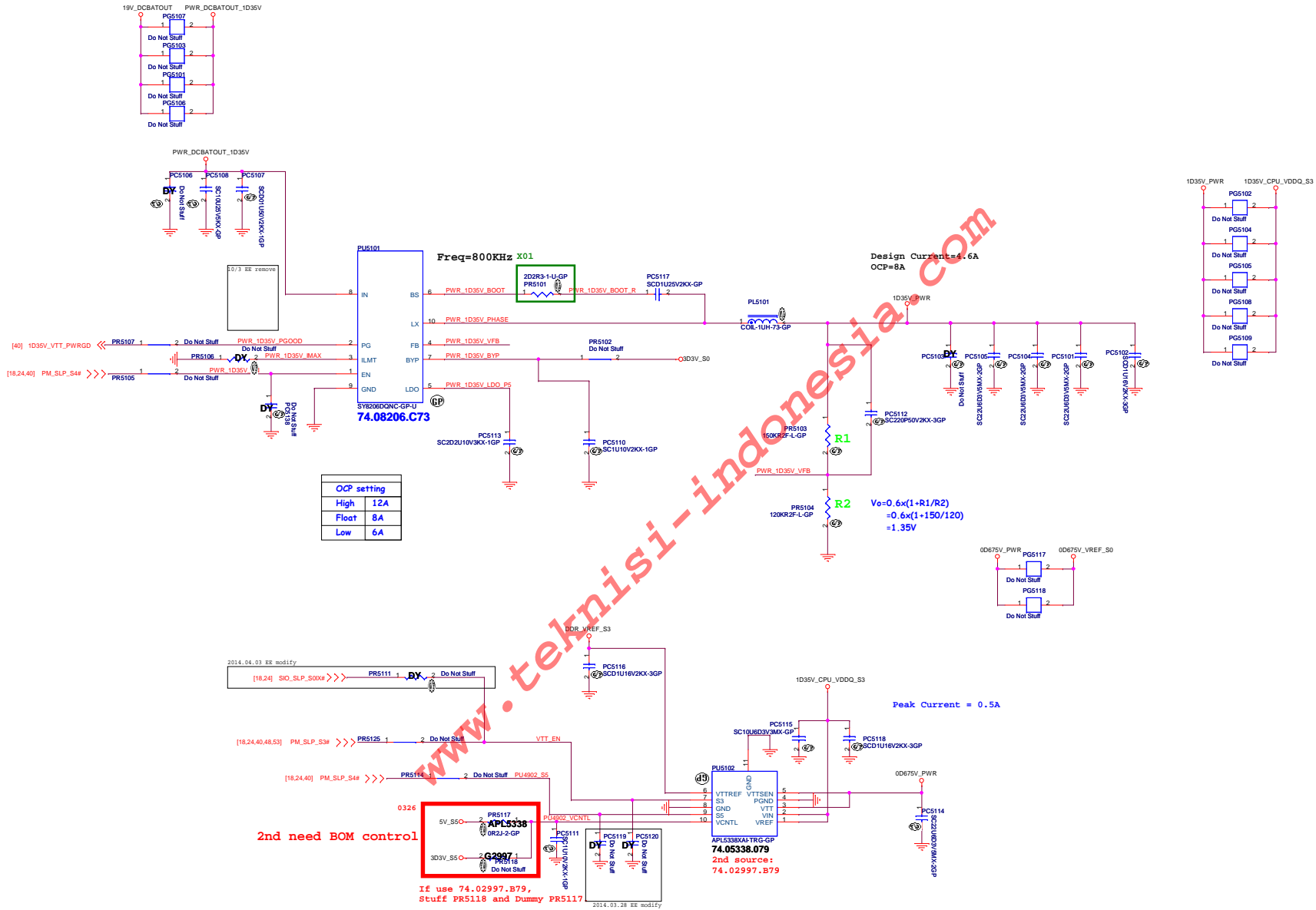
Redwood MLK 1st



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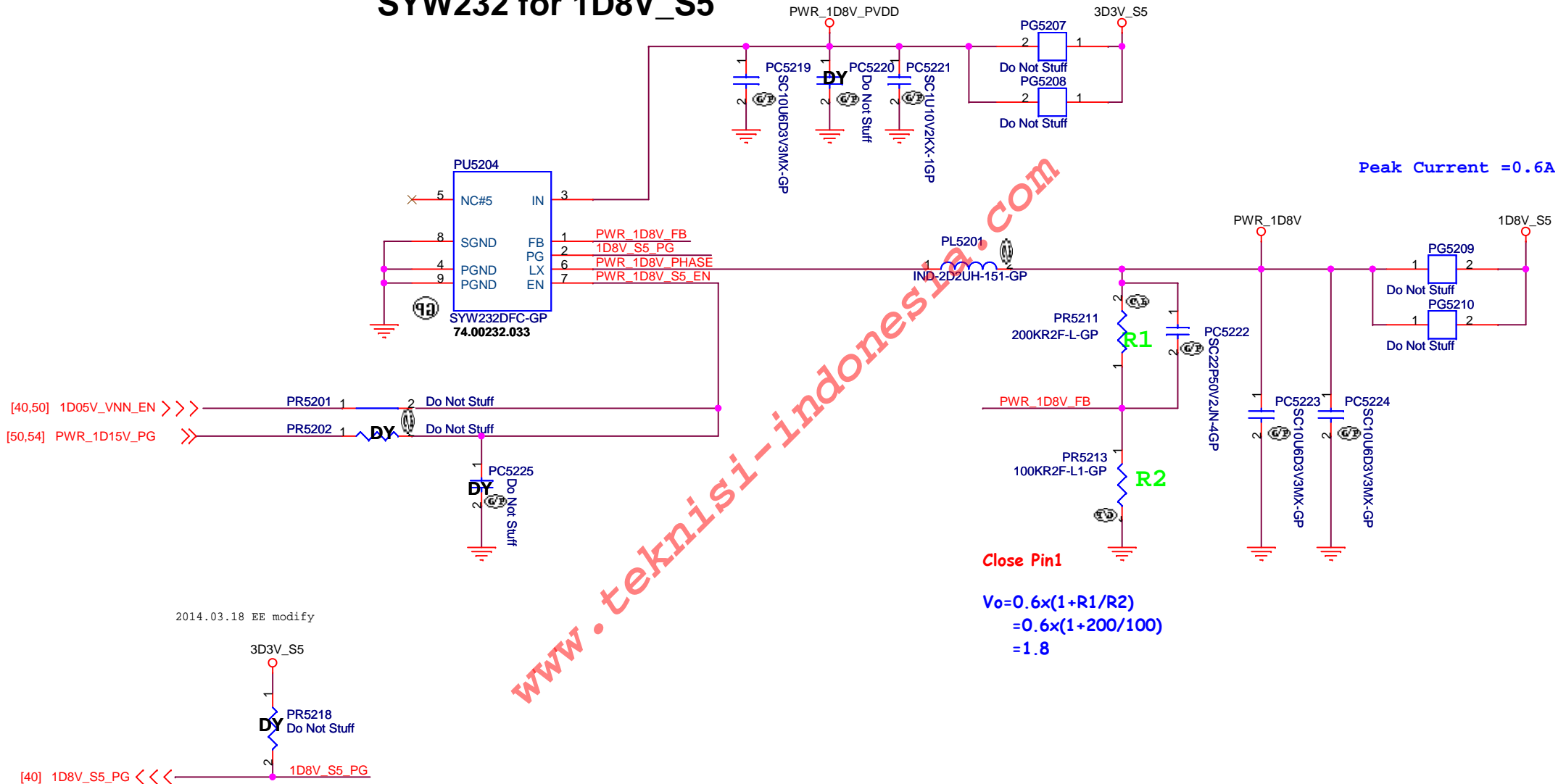
Title		
DCDC VNN 1D05V 1D15V		
Size	Document Number	Rev
A3	Redwood BSW 11.6"	A00
Date:	Wednesday, March 25, 2015	Sheet 50 of 109

SY8206D for 1D35V



SSID = PWR.Plane.Regulator_1p8v

SYW232 for 1D8V_S5



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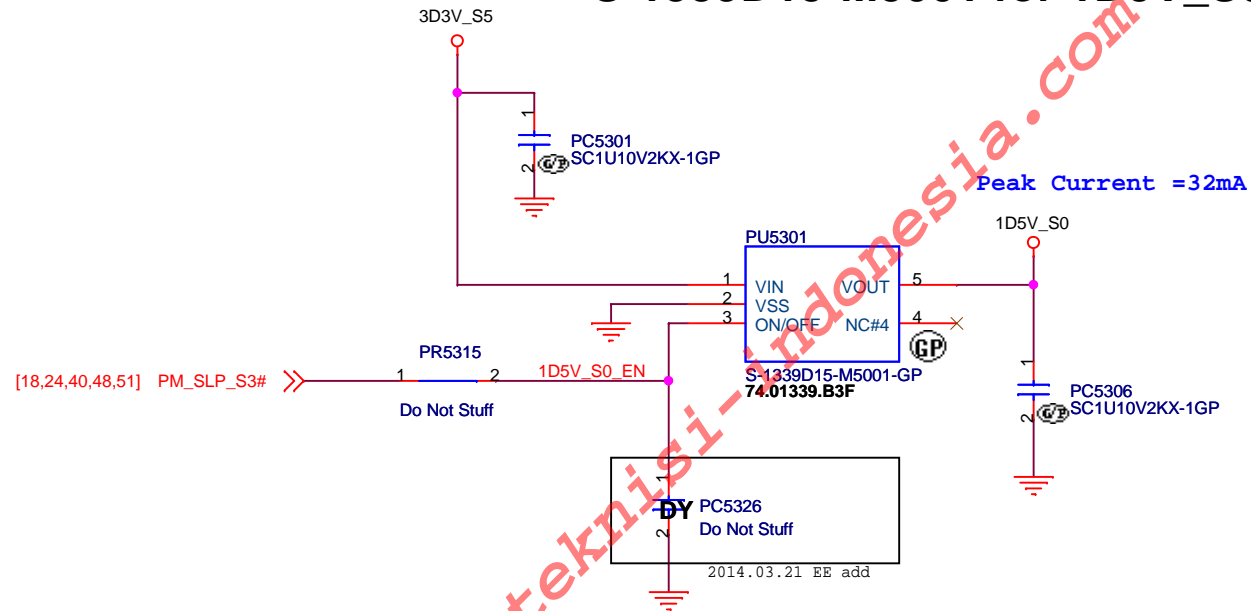


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Title			SYW232DFC_1D8V	
Size	Document Number	Redwood BSW 11.6"		Rev
A4				A00
Date: Wednesday, March 25, 2015		Sheet	52	of 109

S-1339D15-M5001 for 1D5V_S0



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Title

S1339D15 1D5V

Size
A4

Document Number

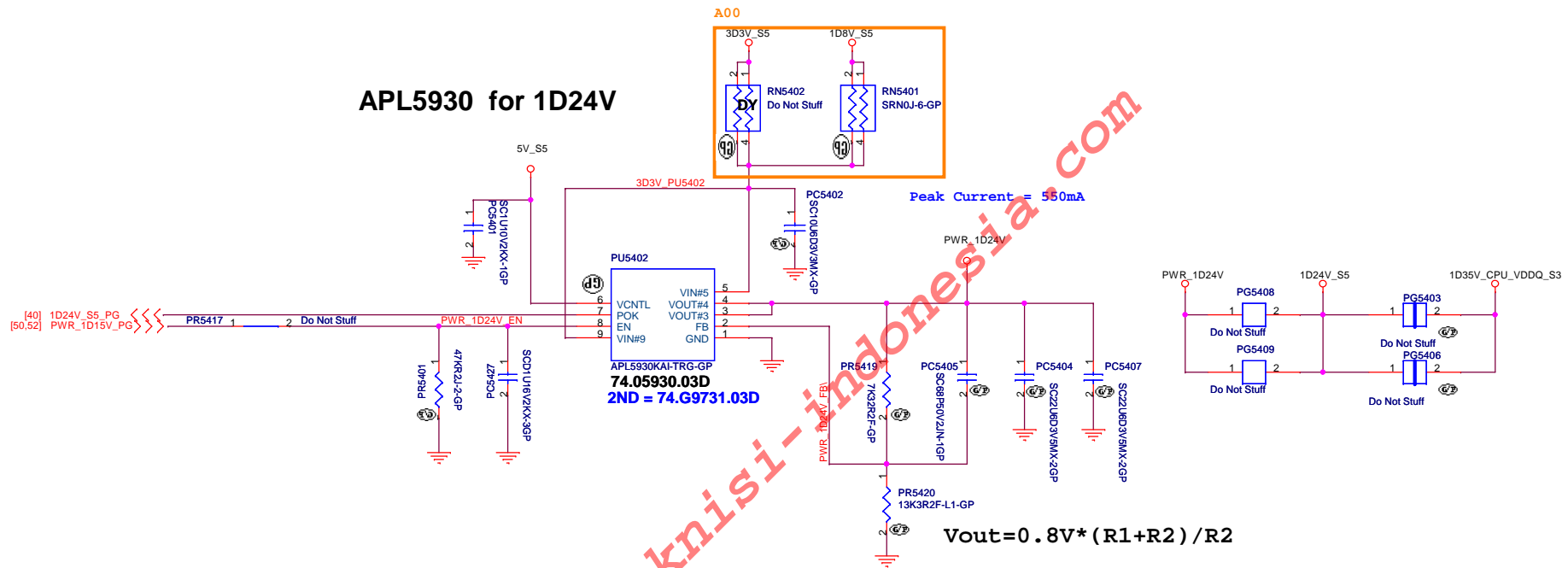
Redwood BSW 11.6"

Rev
A00

Date: Wednesday, March 25, 2015

Sheet 53 of 109

APL5930 for 1D24V

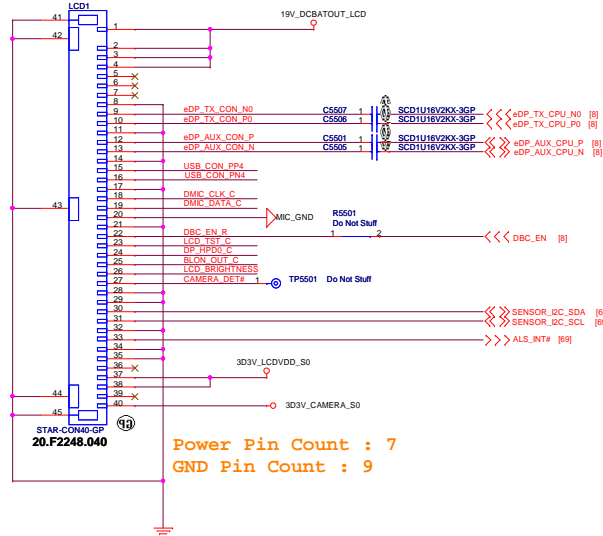


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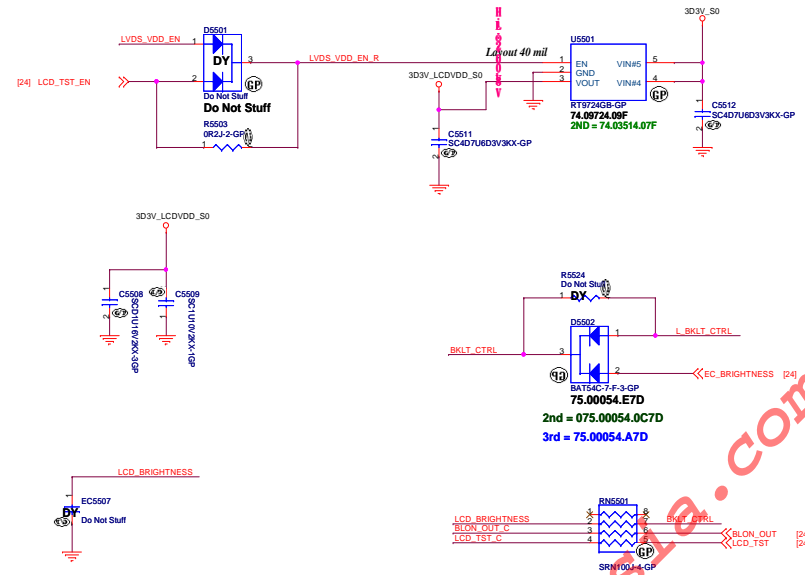


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Size	Document Number	Rev		
A3	Redwood BSW 11.6"	A00		
Date:	Wednesday, March 25, 2015	Sheet	54	of 109

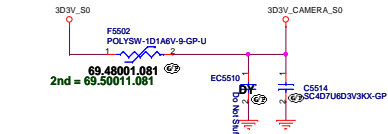
Panel Conn.



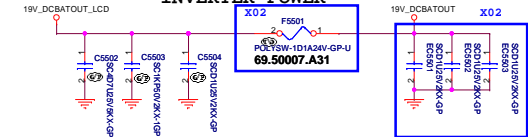
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Power Pin Count : 7
GND Pin Count : 9
```



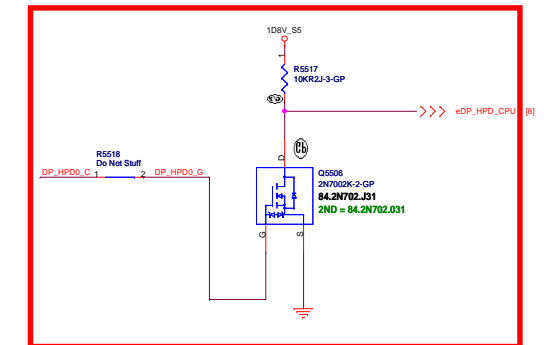
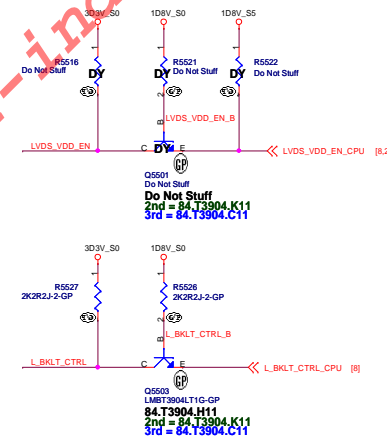
CAMERA POWER



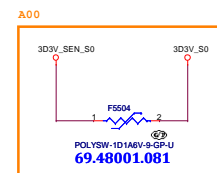
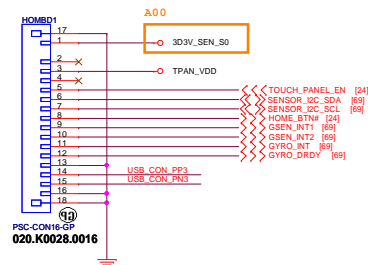
INVERTER POWER



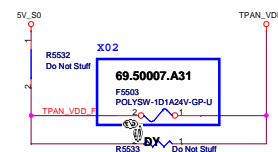
Level shift



[To Home board](#)



TOUCH PANEL POWER



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Title			(Reserved)		
Size	Document Number				Rev
A4	Redwood BSW 11.6"				A00
Date: Thursday, March 19, 2015		Sheet 56 of		109	

SSID = Display Port

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Title (Reserved) Display Port			
Size	Document Number Redwood BSW 11.6"		Rev A00
Date: Thursday, March 19, 2015		Sheet 58 of	109

SSID = DVI

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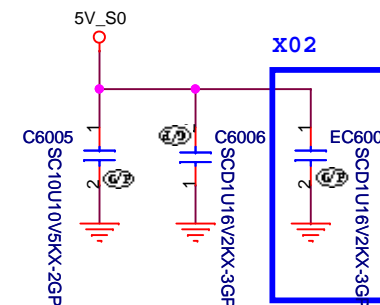
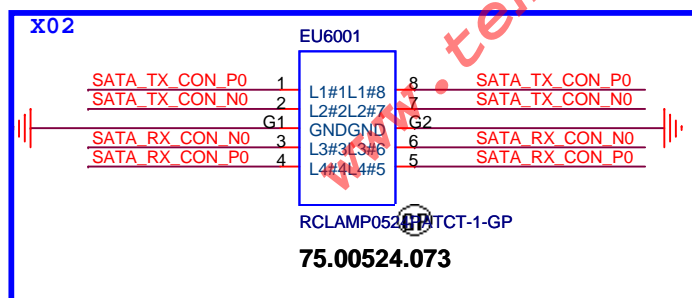
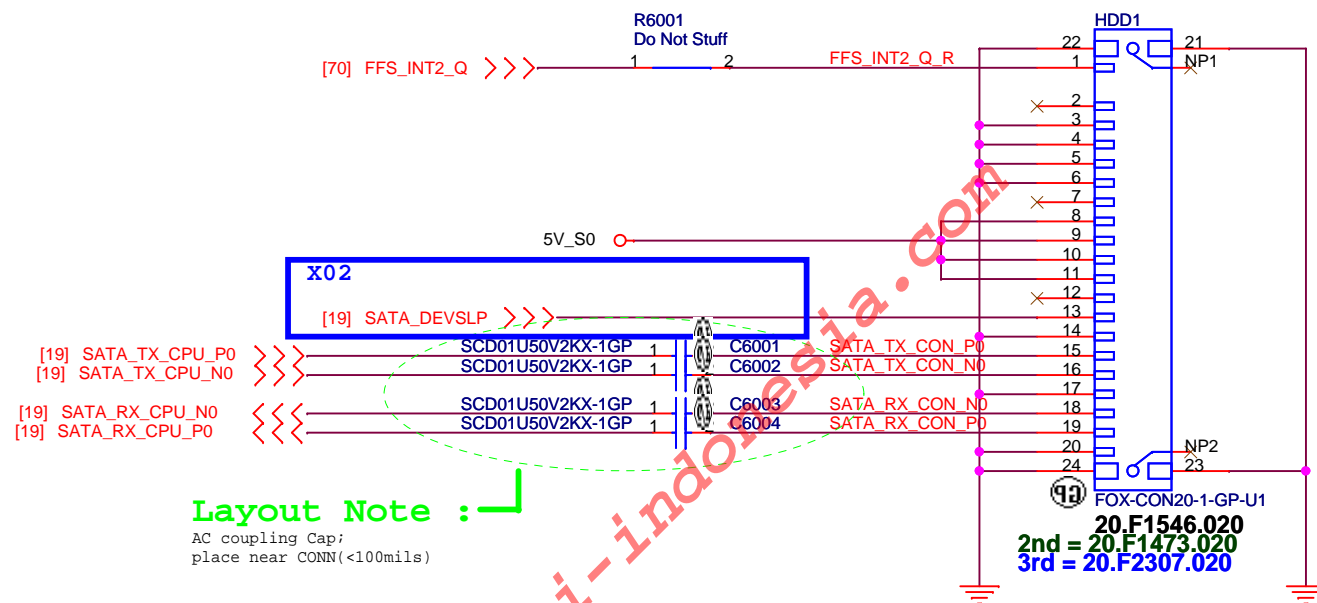
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Title (Reserved) DVI

Size	Document Number	Rev
	Redwood BSW 11.6"	A00

SSID = SATA

SATA HDD Connector



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Title

HDD

Size

Document Number

Redwood BSW 11.6"

Rev

A00

Date: Wednesday, March 25, 2015

Sheet 60 of 109

SSID = WLAN

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(Reserved) WLAN

Size

Document Number

Rev

Redwood BSW 11.6"

A00

Date: Thursday, March 19, 2015

Sheet 61 of 109

SSID = WWAN

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(Reserved) WWAN

Size

Document Number

Redwood BSW 11.6"

Rev

A00

Date: Thursday, March 19, 2015

Sheet 62 of 109

SSID = SSD-NGFF

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Title (Reserved) SSD-NGFF

Size A4	Document Number Redwood BSW 11.6"	Rev A00
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SSID = LED / PWRBTN

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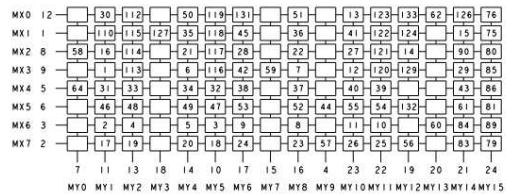
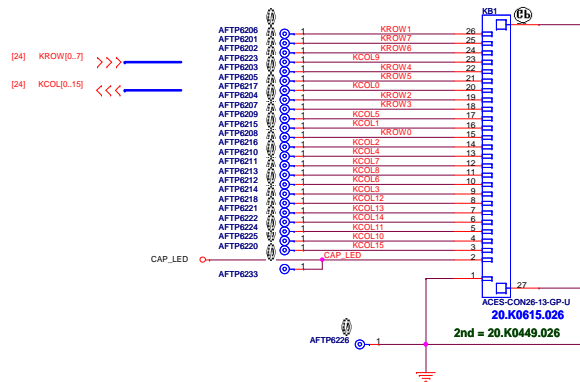
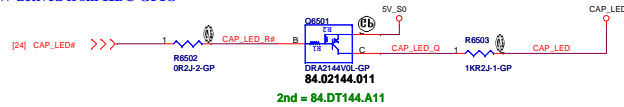
Title **(Reserved) LED / PWRBTN**

Size A4	Document Number Redwood BSW 11.6"	Rev A00
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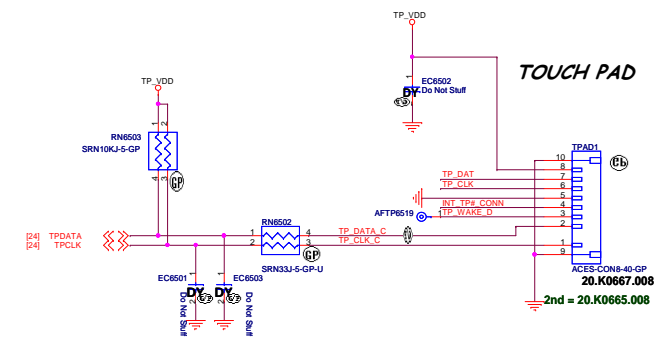
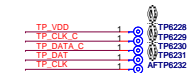
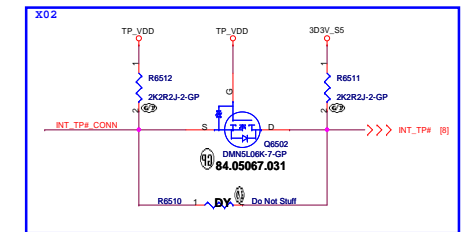
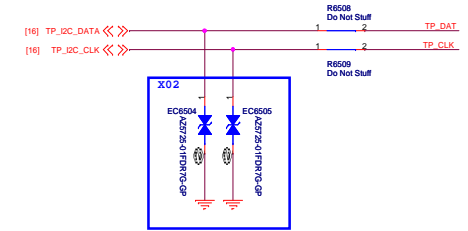
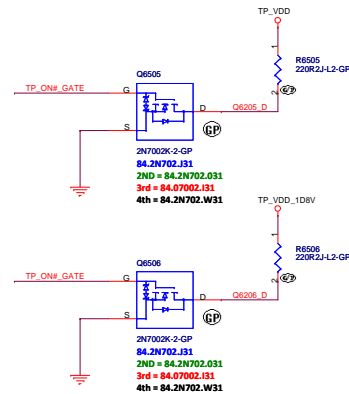
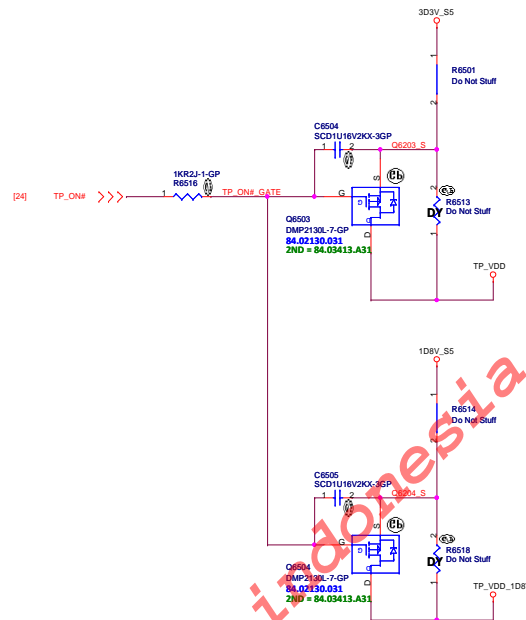
Date: Thursday, March 19, 2015 Sheet 64 of 109

SSID = KB / TOUCH PAD

CAP LED Control
LOW actived from KBC GPIO

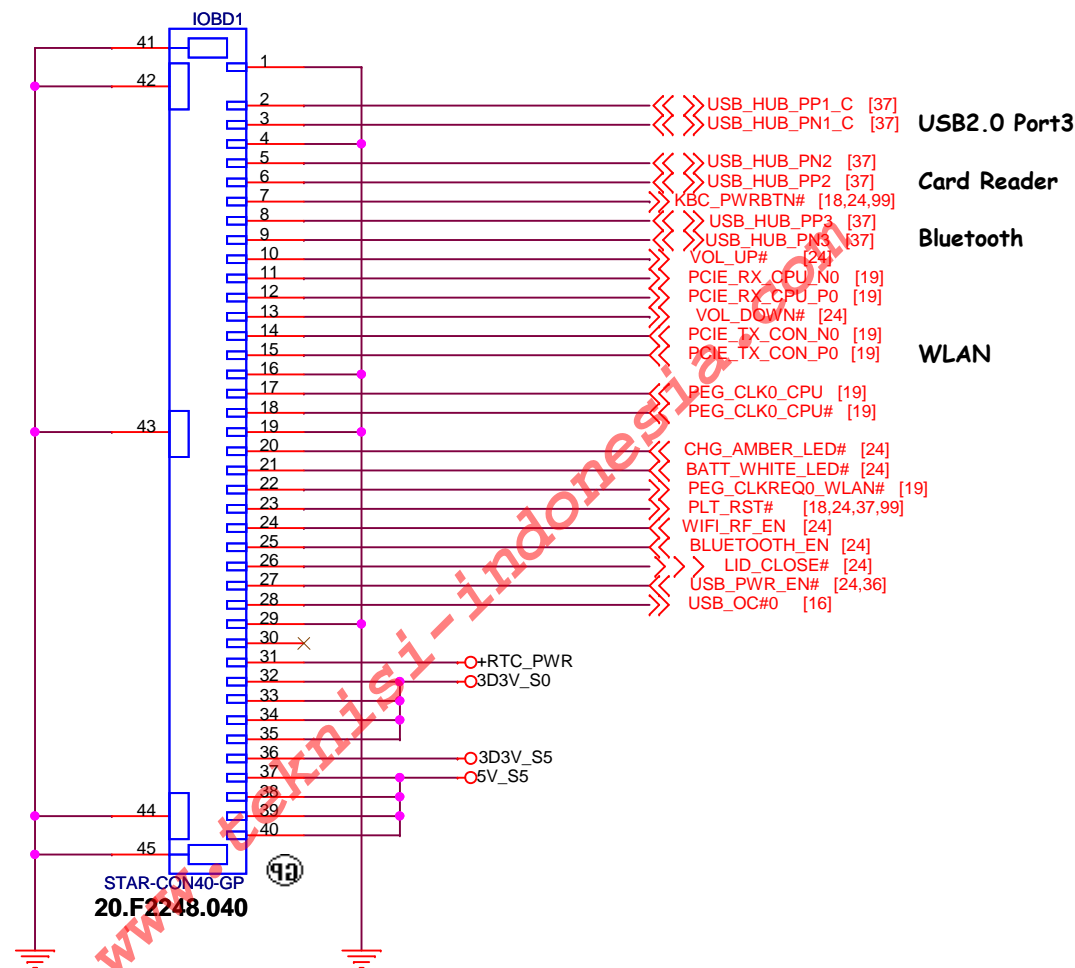


Pin	Signal
1	KS11
2	KS17
3	KS16
4	KS09
5	KS14
6	KS15
7	KS00
8	KS12
9	KS13
10	KS05
11	KS01
12	KS10
13	KS02
14	KS04
15	KS07
16	KS08
17	KS06
18	KS03
19	KS012
20	KS013
21	KS014
22	KS011
23	KS010
24	KS015
25	LED+
26	LED-



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Power Pin Count : 10
GND Pin Count : 5

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Title

IO Board CONN

Size
A4

Document Number

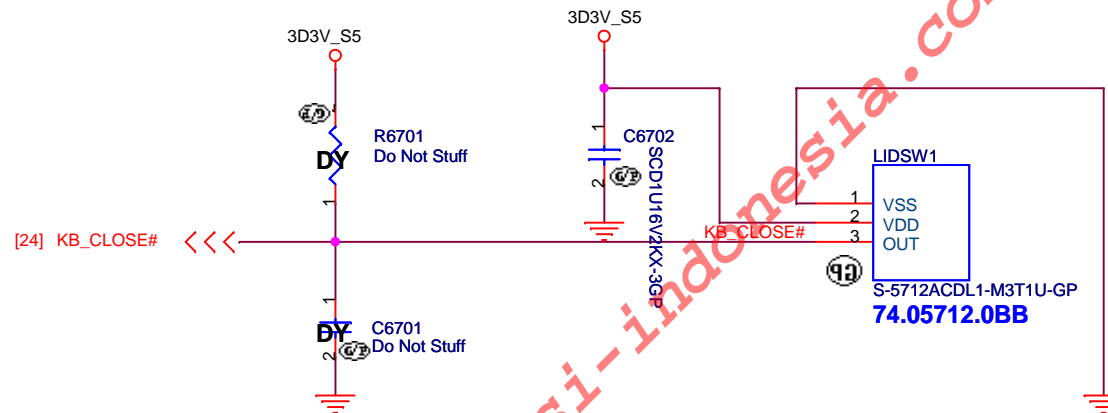
Redwood BSW 11.6"

Rev

A00

Date: Wednesday, March 25, 2015

Sheet 66 of 109



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Title

Hall Sensor

Size
A4

Document Number

Redwood BSW 11.6"

Rev
A00

Date: Wednesday, March 25, 2015


Sheet 67 of 109

SSID = Debug CONN

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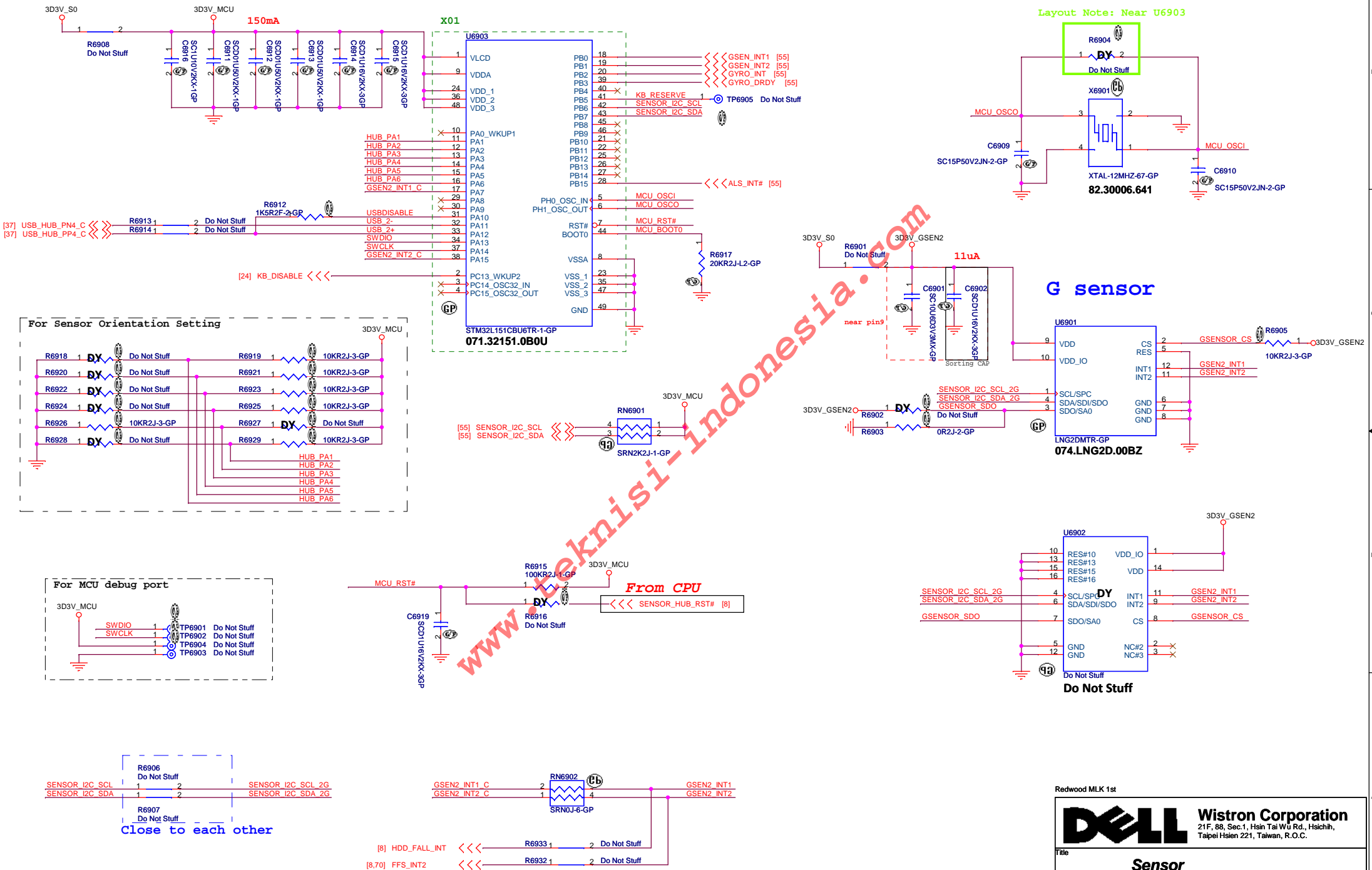
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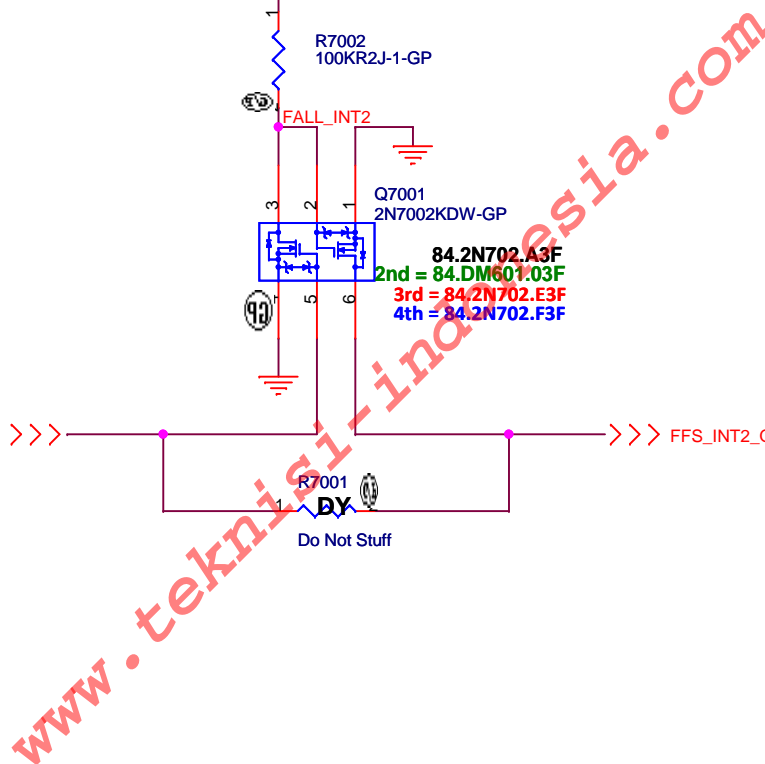
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <i>(Reserved) Debug CONN</i>			
Size A4	Document Number <i>Redwood BSW 11.6"</i>		Rev <i>A00</i>
Date: Thursday, March 19, 2015		Sheet 68	of 109

SSID = Sensor

Sensor Hub



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Free Fall Sensor

Rev
400

Redwood BSW 11.6"

Sheet	70	of	109
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Title **(Reserved)Thunderbolt (1/5)**

Size A4	Document Number Redwood BSW 11.6"	Rev A00
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Date: Thursday, March 19, 2015 Sheet 71 of 109

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Title **(Reserved)Thunderbolt (2/5)**

Size A4	Document Number Redwood BSW 11.6"	Rev A00
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Date: Thursday, March 19, 2015 Sheet 72 of 109

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Title **(Reserved)Thunderbolt (3/5)**

Size A4	Document Number Redwood BSW 11.6"	Rev A00
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Date: Thursday, March 19, 2015 Sheet 73 of 109

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Title **(Reserved)Thunderbolt (4/5)**

Size A4	Document Number Redwood BSW 11.6"	Rev A00
------------	---	-------------------

Date: Thursday, March 19, 2015 Sheet 74 of 109

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Title **(Reserved)Thunderbolt (5/5)**

Size A4	Document Number Redwood BSW 11.6"	Rev A00
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Date: Thursday, March 19, 2015 Sheet 75 of 109

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Title **(Reserved)GPU (1/5) PEG**

Size A4	Document Number Redwood BSW 11.6"	Rev A00
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Date: Thursday, March 19, 2015 Sheet 76 of 109

Blanking

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Title **(Reserved)GPU (2/5) DIGITAL**

Size A4	Document Number Redwood BSW 11.6"	Rev A00
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Date: Thursday, March 19, 2015 Sheet 77 of 109

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Title **(Reserved)GPU (3/5) VRAM**

Size A4	Document Number Redwood BSW 11.6"	Rev A00
------------	---	-------------------

Date: Thursday, March 19, 2015 Sheet 78 of 109

Blanking

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Title **(Reserved)GPU (4/5) GPIO**

Size A4	Document Number Redwood BSW 11.6"	Rev A00
------------	---	-------------------

Date: Thursday, March 19, 2015 Sheet 79 of 109

Blanking

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Title **(Reserved)GPU (5/5) PWR/GND**

Size A4	Document Number Redwood BSW 11.6"	Rev A00
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Date: Thursday, March 19, 2015 Sheet 80 of 109

Blanking

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Title **(Reserved)VRAM1,2 (1/4)**

Size A4	Document Number Redwood BSW 11.6"	Rev A00
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Date: Thursday, March 19, 2015 Sheet 81 of 109

Blanking

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Title **(Reserved)VRAM3,4 (2/4)**

Size A4	Document Number Redwood BSW 11.6"	Rev A00
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Date: Thursday, March 19, 2015 Sheet 82 of 109

Blanking

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Title **(Reserved)VRAM5,6 (3/4)**

Size A4	Document Number Redwood BSW 11.6"	Rev A00
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Date: Thursday, March 19, 2015 Sheet 83 of 109

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Title **(Reserved)VRAM7,8 (4/4)**

Size A4	Document Number Redwood BSW 11.6"	Rev A00
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Date: Thursday, March 19, 2015 Sheet 84 of 109

Blanking

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Title **(Reserved)VGA_CORE**

Size A4	Document Number Redwood BSW 11.6"	Rev A00
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Date: Thursday, March 19, 2015 Sheet 85 of 109

Blanking

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Title **(Reserved)DISCRETE VGAPOWER**

Size	Document Number Redwood BSW 11.6"	Rev A00
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Date: Thursday, March 19, 2015 Sheet 86 of 109

Blanking

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Size
A4

Document Number

Redwood BSW 11.6"

Rev
A00

Date: Thursday, March 19, 2015

Sheet 87 of 109

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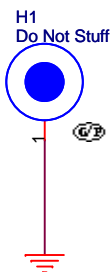
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Title **(Reserved)**

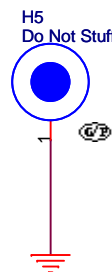
Size A4	Document Number Redwood BSW 11.6"	Rev A00
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Date: Thursday, March 19, 2015 Sheet 88 of 109

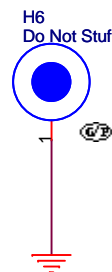
Do Not Stuff



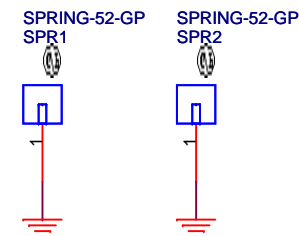
Do Not Stuff



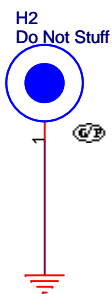
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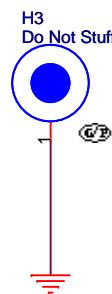
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Do Not Stuff



Do Not Stuff

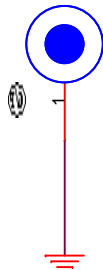


Do Not Stuff



34.4UV01.101

HS1
STF237R128H42-5-GP



34.4UV28.101

34.4UV01.101

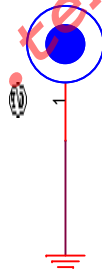
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STF237R128H42-5-GP



34.4UV28.101

34.4UV01.101

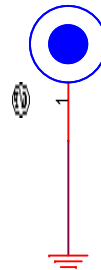
HS3
STF237R128H42-5-GP



34.4UV28.101

34.4UV01.101

HS4
STF237R128H42-5-GP



34.4UV28.101

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Title

UNUSED PARTS/EMI Capacitors

Size
A4

Document Number

Redwood BSW 11.6"

Rev
A00

Date: Thursday, March 19, 2015

Sheet 89 of 109

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Title **(Reserved)NFC Connector**


Size A4	Document Number Redwood BSW 11.6"	Rev A00
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Date: Thursday, March 19, 2015 Sheet 90 of 109

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Size A4	Document Number Redwood BSW 11.6"		Rev A00
Date: Thursday, March 19, 2015		Sheet 91 of	109

Blanking

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Size A4	Document Number Redwood BSW 11.6"		Rev A00
Date: Thursday, March 19, 2015		Sheet 92 of	109

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Title **(Reserved)Express Card**

Size A4	Document Number Redwood BSW 11.6"	Rev A00
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Date: Thursday, March 19, 2015 Sheet 93 of 109

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Title			(Reserved)Smart Card Socket		
Size	Document Number				Rev
A4	Redwood BSW 11.6"				A00
Date: Thursday, March 19, 2015			Sheet	94	of 109

Blanking

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(Reserved)SW GFX eDP

Size
A4

Document Number

Redwood BSW 11.6"

Rev
A00

Date: Thursday, March 19, 2015

Sheet 95 of 109

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(Reserved)Bottom Docking

Size
A4

Document Number

Redwood BSW 11.6"

Rev
A00

Date: Thursday, March 19, 2015

Sheet 96 of 109

Blanking

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Size
A4

Document Number

Redwood BSW 11.6"

Rev
A00

Date: Thursday, March 19, 2015

Sheet 97 of 109

Blanking

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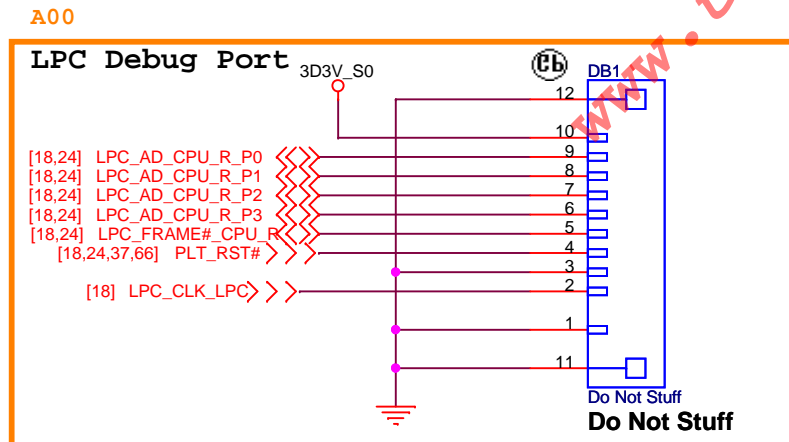
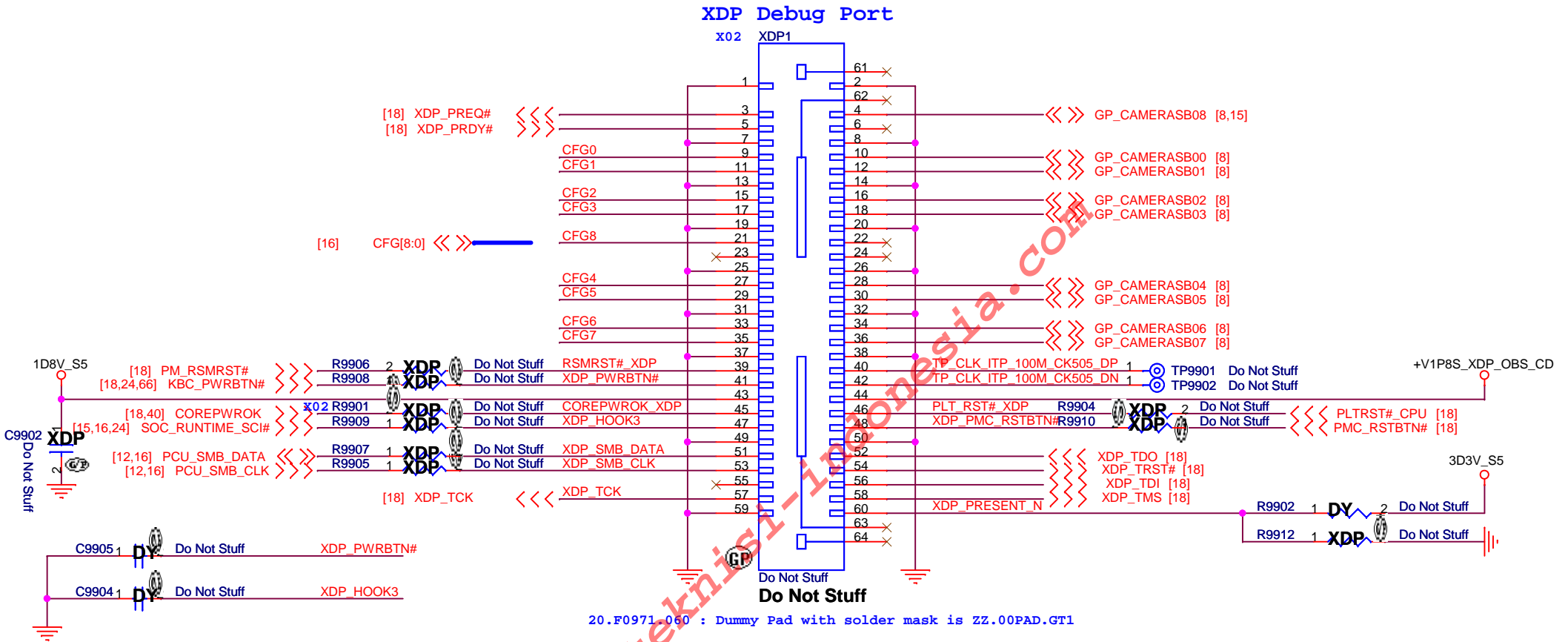
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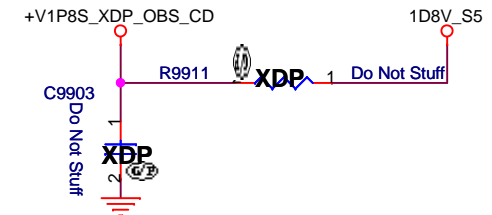
Size	Document Number Redwood BSW 11.6"	Rev A00
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Date: Thursday, March 19, 2015 Sheet 98 of 109

SSID = DEBUG PORT



20.F1180.010: Dummy Pad with solder mask is ZZ.00PAD.GV1



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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of Temperature on the Rate of Reaction	John Doe	2018	Journal of Chemical Education	95	3	456-462
2. Kinetics of the Reaction Between Hydrogen Peroxide and Potassium Iodide	Jane Smith	2017	Journal of Chemical Education	94	2	321-328
3. The Effect of Concentration on the Rate of Reaction	Michael Brown	2016	Journal of Chemical Education	93	1	123-130
4. The Effect of Surface Area on the Rate of Reaction	Sarah White	2015	Journal of Chemical Education	92	4	567-574
5. The Effect of Catalyst on the Rate of Reaction	David Green	2014	Journal of Chemical Education	91	5	678-685

CPU XDP

Redwood BSW 11.6"

Size	A4
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Document Number

Rev
A00

Date: Wednesday, March 25, 2015

Sheet 99 of 109

109

Table 29. Straps (Sheet 1 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDIO Detect	Weak internal pull-down	DDIO Detect 0 = DDIO not detected 1 = DDIO detected
GPIO_SUS[1]	DDI1 Detect	Weak internal pull-down	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	A16 swap overdrive	Weak internal pull-up	Top Swap (A16 Override) 0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[4]	Boot BIOS Strap BBS	Weak internal pull-up	BIOS Boot Selection 0 = - 1 = SPI
GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal pull-up	Security Flash Descriptors 0 = Override 1 = Normal Operation

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[8]	ICLK, USB2, DDI SFR Supply Select	Weak internal pull-down	0 = Supply is 1.25V 1 = Supply is 1.35V This strap also contains PLL LDO 0: supply is 1.25V; 1: supply is 1.35V. Selects supply voltage for LDOs used for PLLs, thermal oscillators, USB2, ICLK and DDI
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal pull-up	0 = No bypass 1 = Bypass with 1.05V
GPIO_SUS[10]	POSM Select	Weak internal pull-down	Selects which POSM will be observed at time 0 0 = Fuse controller 1 = PMC
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass

CHV Straps [CRB] -- strap detect @ RSMRST# assertion				
Purpose	CHV Pin Name (refer CHV symbol PIN)	PU/PD (internal - Weak)	Options	Default State on board?
DSI Display Detected	GPIO_SUS3	PD	1 - DSI detect, 0 - Disable	Low
DFX Boot Halt Strap & VISA Early POSM Debug Enable	GPIO_SUS6	PU	1 - normal, 0 - Halt boot enable	High
DFX Sus Debug Strap	GPIO_SUS7	PU	1 - Normal, 0 - Sus Debug enable	High

USB2.0 MCP Side

Pair	Device
0	USB port 1 (usb charger)
1	USB port 2
2	USB HUB
3	Touch Panel
4	CAMERA

USH Side

Pair	Device
0	NA
1	NA

USB HUB Side

Pair	Device
1	USB2.0 Port3
2	Card Reader
3	Bluetooth
4	Sensor Hub

USB3.0 MCP Side

Pair	Device
1	USB port 1
2	USB port 2
3	N/A
4	N/A

PCIE Table

PCIE	
Lane	Device
1	WLAN
2	NA
3	NA
4	NA

SATA Table

SATA	
Pair	Device
0	HDD
1	NA

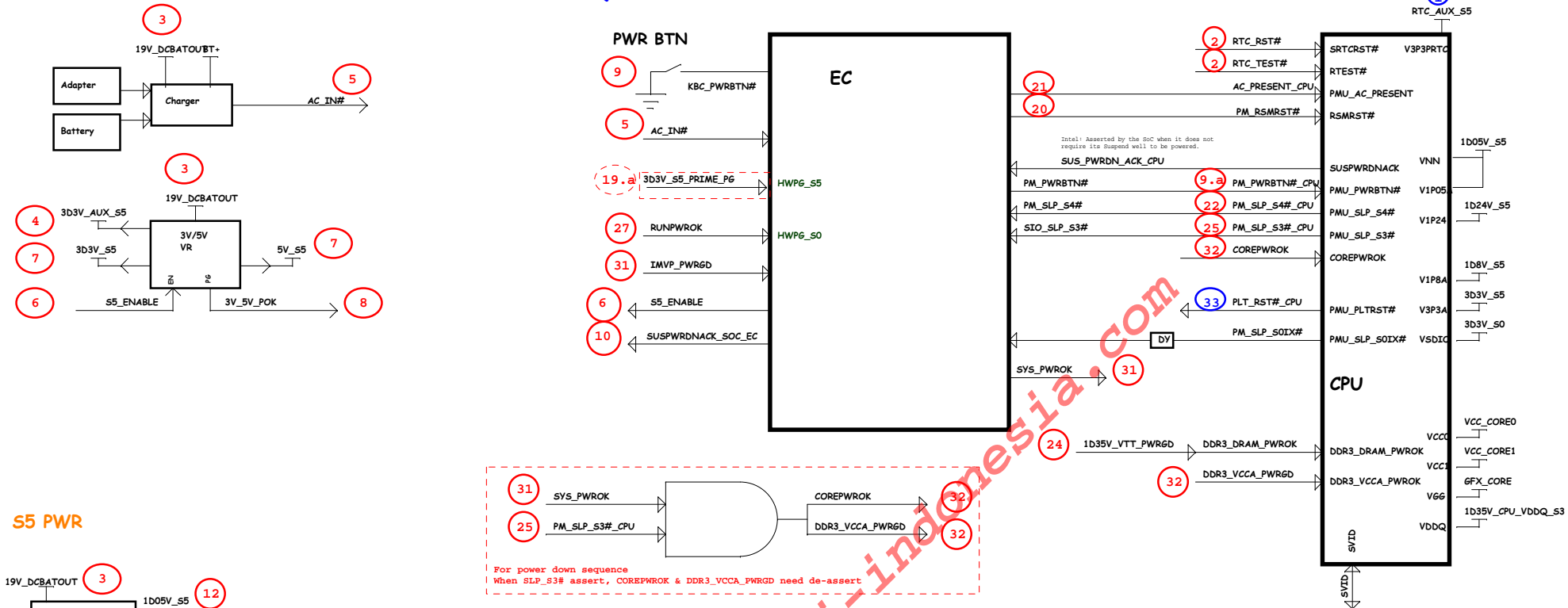
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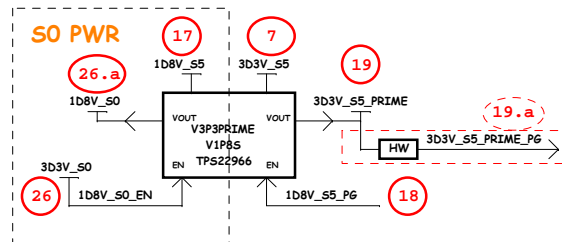
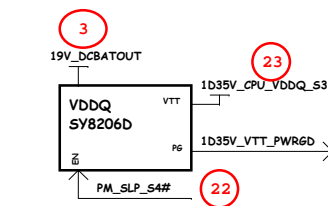
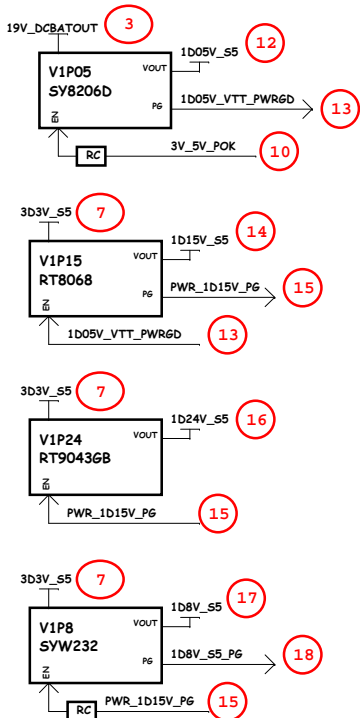
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Table of Content		
Size A3	Document Number Redwood BSW 11.6"	Rev A00
Date: Thursday, March 19, 2015	Sheet 100	of 109

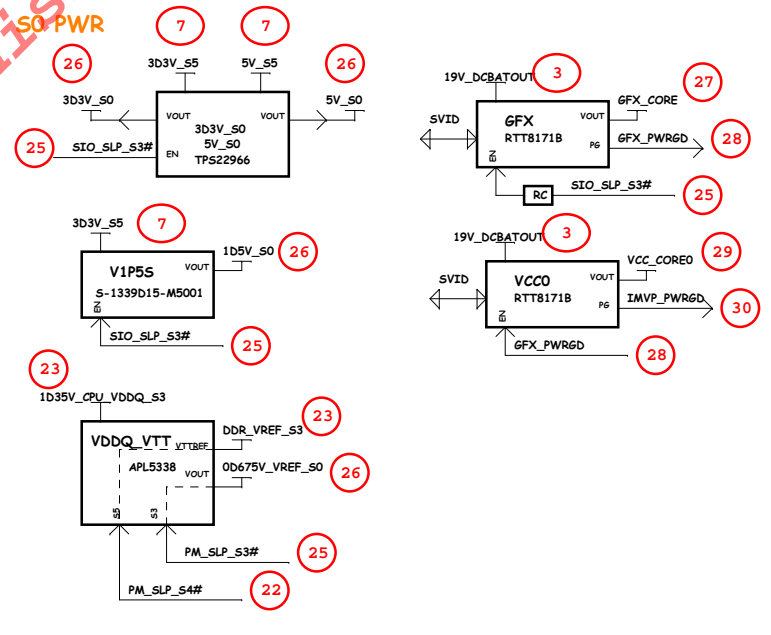
Braswell POWER UP SEQUENCE DIAGRAM



S5 PWR



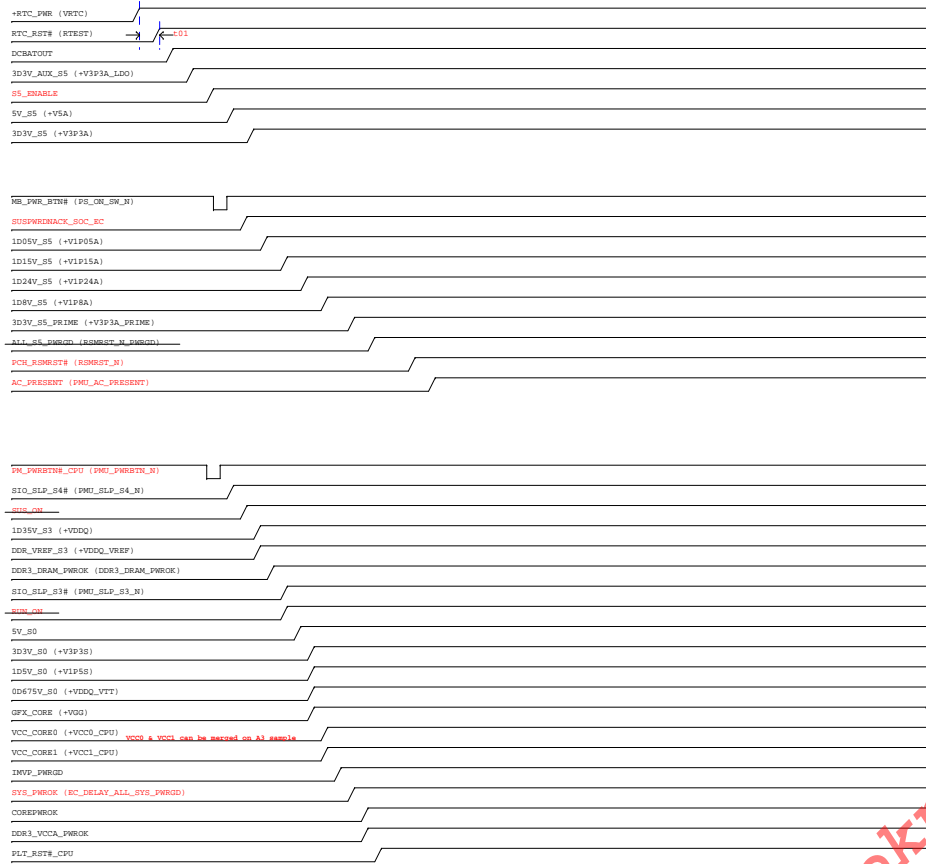
S0 PWR



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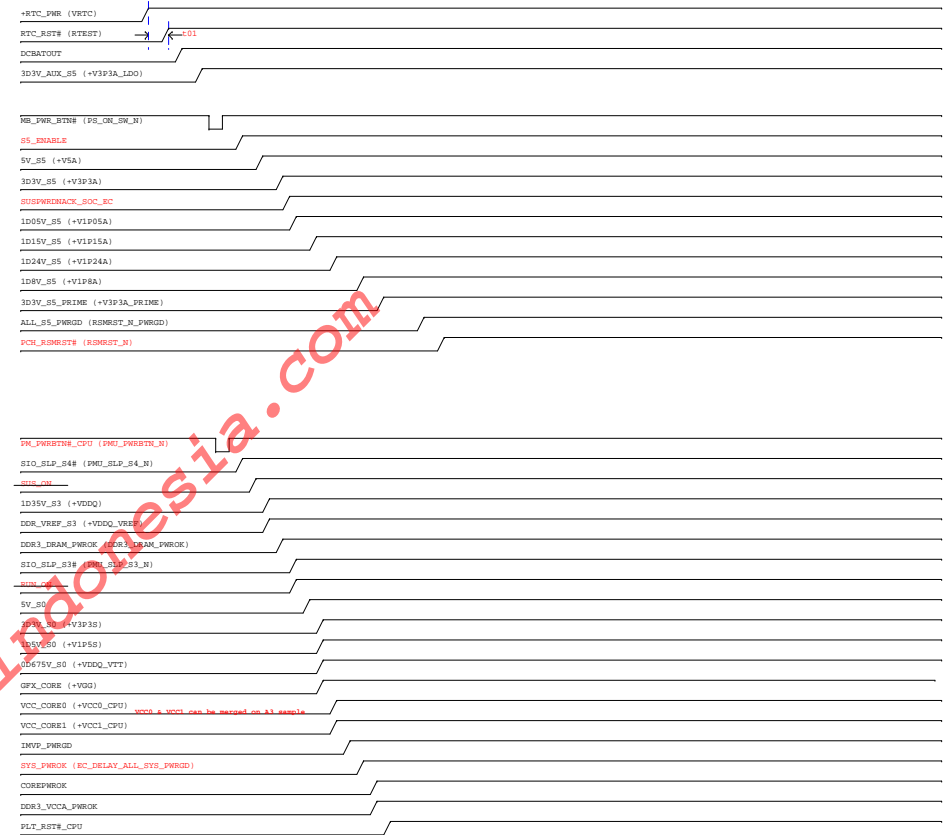
Intel-Power Up Sequence

(AC mode) Red word : RBC GP20



Intel-Power Up Sequence

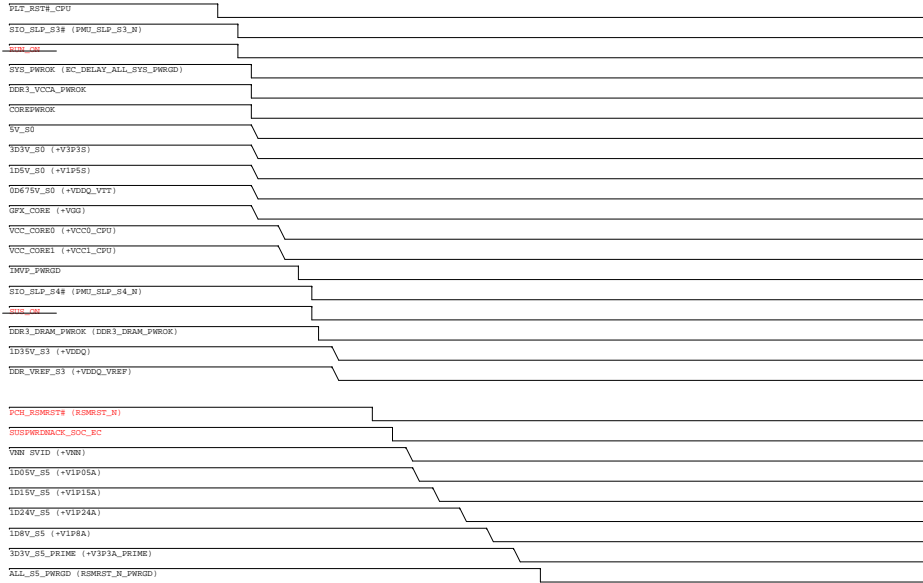
(DC mode) Red word : RBC GP20



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Intel-Power Down Sequence

(AC mode) Red word : KBC GPIO



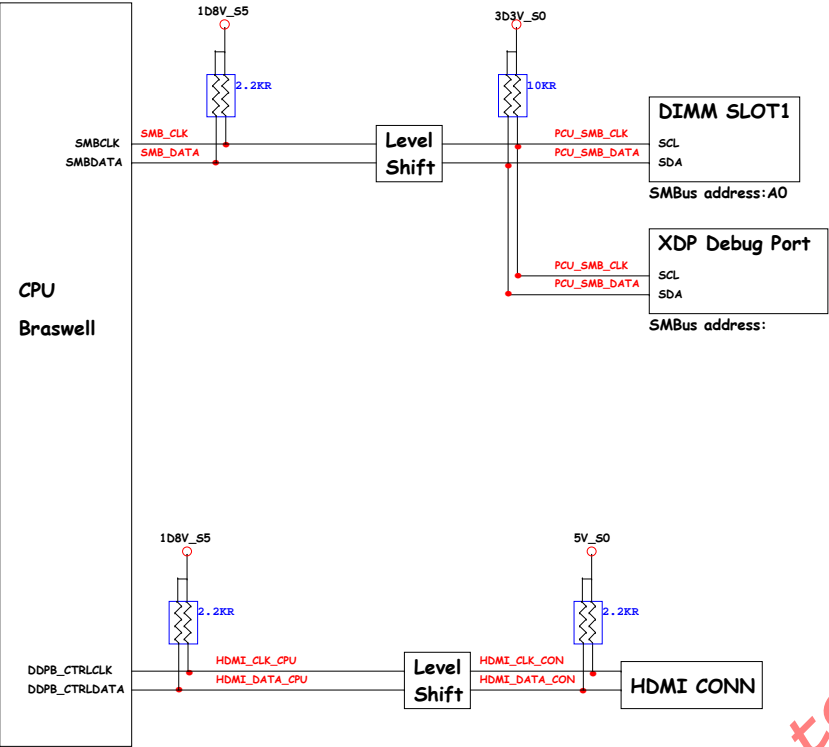
Intel-Power Down Sequence

(DC mode) Red word : KBC GPIO

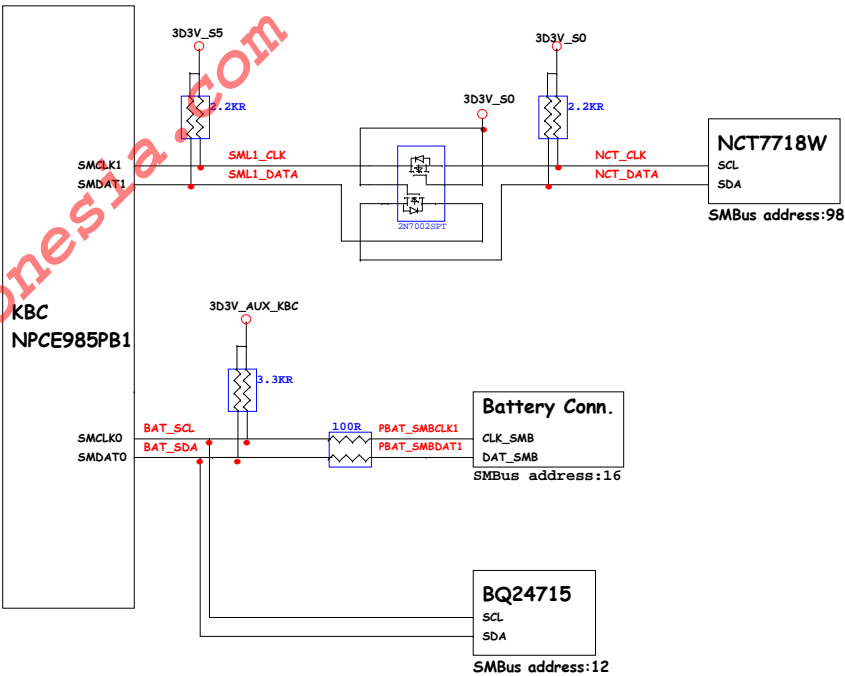


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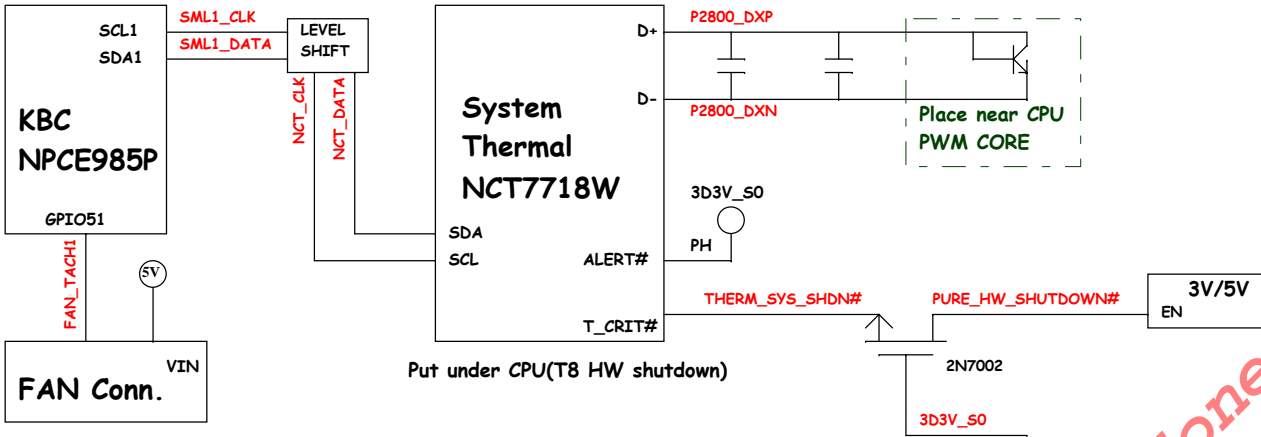
PCH SMBus Block Diagram



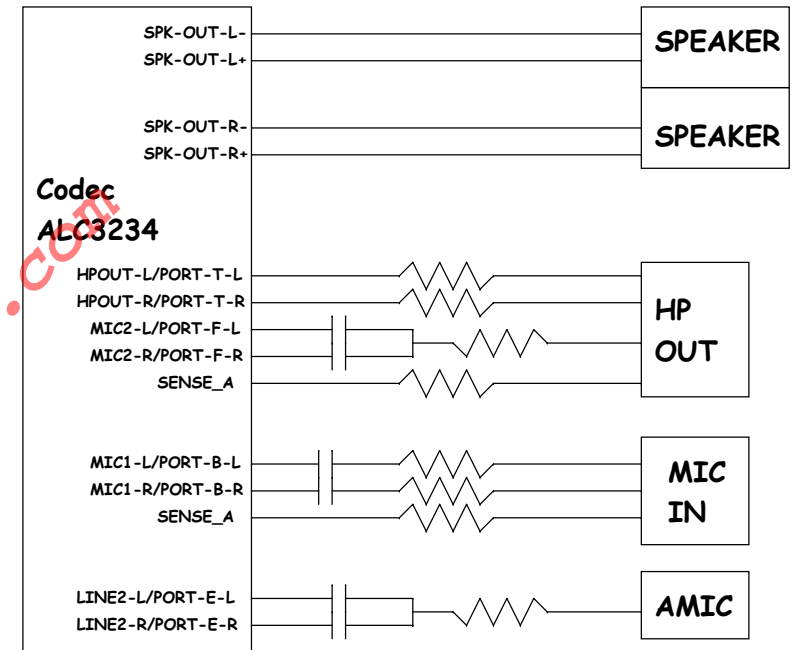
KBC SMBus Block Diagram



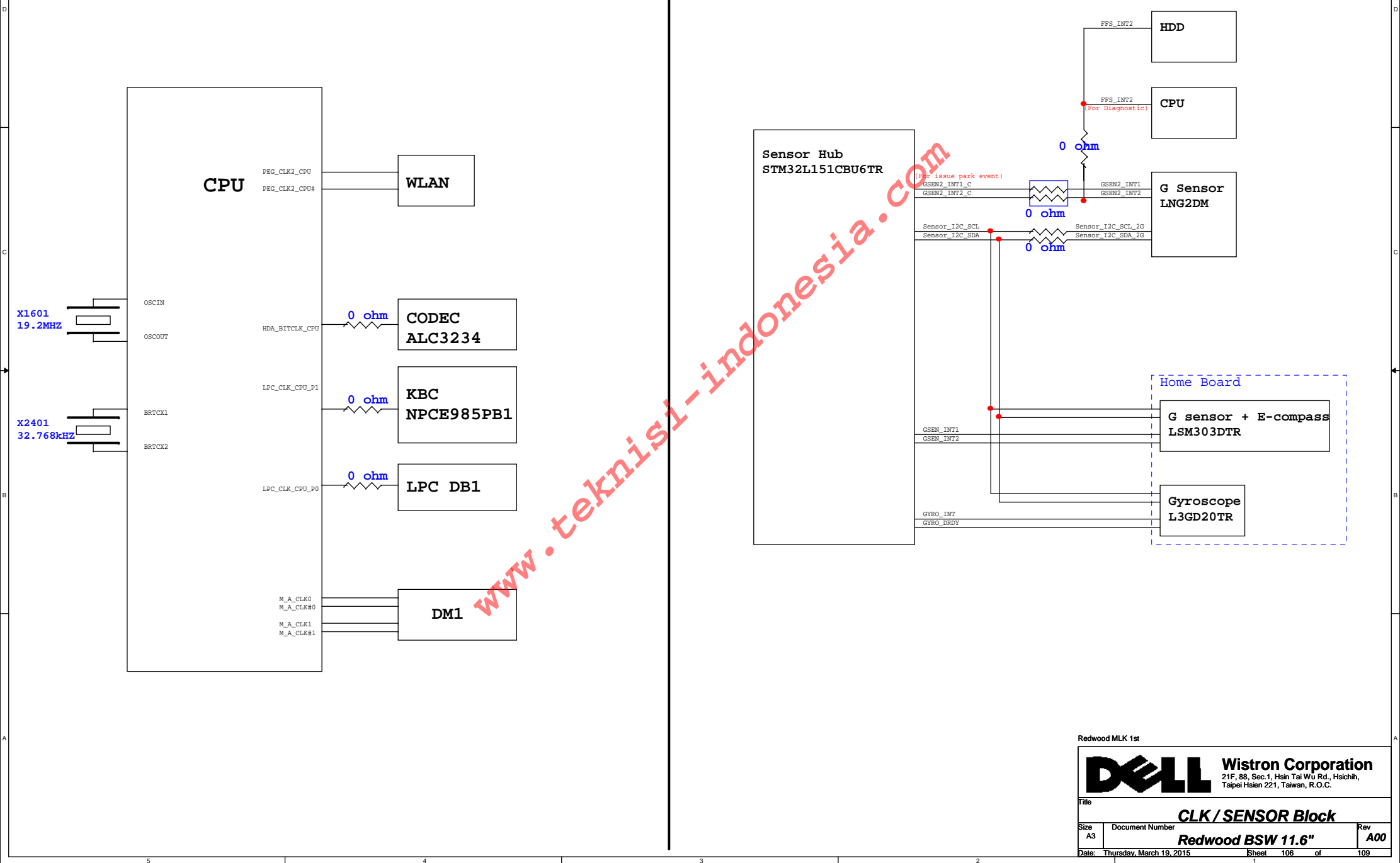
Thermal Block Diagram



Audio Block Diagram



SSID = CLK Block Diagram



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Title

CLK / SENSOR Block

Size
A3

Document Number

Redwood BSW 11.6"

Rev

A00


Date: Thursday, March 19, 2015

Sheet 106 of 109

Item	Page#	Date	Request By	Issue description					Solution Description					Rev.					
1																			
2																			
3																			
4																			
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Change History-01

Size

Document Number

Rev

A00

Date: Thursday, March 19, 2015

Sheet 107 of 109

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
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Size

Document Number

Rev

Redwood BSW 11.6"

A00

Date: Thursday, March 19, 2015

Sheet 108 of 109

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